
STPC[®] Consumer-II Programming Manual

Issue 1.2

February 8, 2002



STMicroelectronics

Information provided is believed to be accurate and reliable. However, ST Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringements of patents or other rights of third parties which may result from its use. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied.

1 TABLE OF CONTENTS

TABLE OF CONTENTS	3
LIST OF TABLES	7
LIST OF FIGURES	9
INTRODUCTION	11
HOW TO USE THIS MANUAL	13
5.1. INTRODUCTION	13
5.2. SPECIFIC NOTES	13
5.3. ISSUING NOTES	15
LIST OF REGISTERS	17
HOST INTERFACE	29
7.1. INTRODUCTION	29
7.2. AGENT DECODING	31
7.3. MEMORY ADDRESS MAP	31
7.4. IO ADDRESS MAP	35
7.5. CACHE RELATED REGISTERS	36
7.6. ADDRESS DECODE RELATED REGISTERS	42
7.7. HOST SDRAM CONTROLLER REGISTERS	49
7.8. ACCESSING CONFIGURATION REGISTERS	53
SDRAM Controller	55
8.1. INTRODUCTION	55
8.2. MEMORY CONTROLLER	55
8.3. SDRAM REGISTER ACCESS	56
8.4. MEMORY CLOCK REGISTERS	60
8.5. SDRAM ARBITRATION:	62
PCI CONTROLLERS	63
9.1. INTRODUCTION	63

TABLE OF CONTENTS

9.2. ACCESSING THE PCI CONFIGURATION REGISTERS	64
9.3. CONFIGURATION ADDRESS REGISTER	65
9.4. CONFIGURATION DATA REGISTER	66
9.5. NORTH BRIDGE CONFIGURATION REGISTERS	66
9.6. THE SOUTH BRIDGE	74
9.7. SOUTH BRIDGE PCI FUNCTION 0 (PCI TO ISA) CONFIGURATION REGISTERS	75
9.8. SOUTH BRIDGE PCI FUNCTION 1 CONFIGURATION REGISTERS	82
ISA INTERFACE	103
10.1.INTRODUCTION	103
10.2.PCI / ISA CYCLES	103
10.3.XBUS READ AND WRITE	106
10.4.ISA STANDARD REGISTERS	108
10.5.ISA CONFIGURATION REGISTERS	116
IDE CONTROLLER	125
11.1.INTRODUCTION	125
11.2.PRD TABLE ENTRY	126
11.3.IDE BUS MASTER REGISTERS	127
11.4.BUS MASTER IDE REGISTER DESCRIPTION	128
11.6.BUS MASTER IDE COMMAND REGISTER	129
11.8.OPERATION	133
11.9.DATA SYNCHRONIZATION	133
11.10.ERROR CONDITIONS	134
11.11.PCI SPECIFICS	135
VGA CONTROLLER	137
12.1.INTRODUCTION	137
12.2.VGA CONTROLLER	137
12.3.VGA REGISTERS	138
12.4.GENERAL VGA REGISTERS	138

TABLE OF CONTENTS

12.5.VGA SEQUENCER REGISTERS	146
12.6.GRAPHICS CONTROLLER REGISTERS	154
12.7.ATTRIBUTE CONTROLLER REGISTERS	165
12.8.CRT CONTROLLER REGISTERS	172
12.9.VGA EXTENDED REGISTERS	202
12.10.ADDITIONAL MODES	233
12.11.INTERLACED MONITOR SUPPORT	233
12.12.RAMDAC REGISTERS	235
12.13DCLK CONTROL REGISTERS	240
GRAPHICS ENGINE	249
13.1.INTRODUCTION	249
13.2.MEMORY ADDRESS SPACE	249
13.3.DUMB FRAME BUFFER ACCESS	250
13.4.ADDRESSING	251
13.5.VGA OPERAND SOURCES	251
13.6.VGA OPERAND FRAME BUFFER ADDRESSES	252
13.7.DRAWING ENGINE REGISTERS	254
13.8.REGISTER ACCESS	255
13.9.REGISTER SPECIFICATION	256
13.10.GE OPERATIONS	278
13.11.CURSOR SUPPORT	289
VIDEO INPUT PORT	301
14.1.INTRODUCTION	301
14.2.VIDEO INPUT PORT (VIP) OVERVIEW	301
14.3.DIGITAL VIDEO INPUT FORMATS	301
14.4.VIP SPECIFICATIONS NOT SUPPORTED	303
14.5.VIDEO INPUT MODULE ADDRESS SPACE	303
14.6.VIP VIDEO INPUT PORT REGISTERS	304

TABLE OF CONTENTS

VIDEO PIPELINE REGISTERS	321
15.1.INTRODUCTION	321
15.2.VIDEO PIPELINE REGISTER LOCATIONS	321
15.3.SOURCE SPECIFICATION REGISTERS	322
15.4.DESTINATION SPECIFICATION REGISTERS	327
15.5.FILTER CONTROL REGISTERS	329
15.6.VIDEO AND GRAPHICS MIXING CONTROL REGISTERS	332
TV OUTPUT PORT	337
16.1.INTRODUCTION	337
16.2.FUNCTIONAL DESCRIPTION	337
16.3.TV OUTPUT PORT REGISTER ACCESS	348
16.4.TV OUTPUT PORT REGISTERS	349
16.6.TV OUTPUT PORT REGISTER CONTENTS AND DESCRIPTION	351
LOCAL BUS INTERFACE	375
17.1.INTRODUCTION	375
17.2.LOCAL BUS REGISTERS	375
17.3.LOCAL BUS ADDRESS DECODE REGISTERS	376
17.4.LOCAL BUS TIMING REGISTERS	382
17.5.LOCAL BUS CONTROL REGISTER	388
17.6.CHIP SELECT MEMORY MAP	390
POWER MANAGEMENT	393
18.1.INTRODUCTION	393
18.2.POWER MANAGEMENT CONTROLLER REGISTERS	395

2 LIST OF TABLES

CPU Registers located in the ST 486 Programming Manual	28
Register CF8h	64
Register CFCh	64
North Bridge Reset Values	66
Function 0 (ISA Bridge) Configuration Space Register Reset Values	75
Function 1 (IDE Bridge) PCI Configuration Space Register Reset Values	82
Operating Mode of the Secondary Channel	88
Operating Mode of the Primary Channel	88
Timing Register Location	98
DMA Speed Mode Select	99
IDE DMA Recovery Time Settings	99
IDE DMA Active Time Settings	100
Recovery R/W Signal Time	100
Active R/W Signal Time	100
Address Setup Time	100
Prefetch Encoding	100
TV Output Port Register/Bit Mapping	349
Activity Detected	394
Suspend Timer Reset	395
Standby Timer Reset	396
House-keeping Timer Reset	397
Peripheral Timer Reset	398
Doze Timer Reset	399
PMU State	418
Power-on and Housekeeping States	421
Doze/Standby/Suspend States	422

LIST OF TABLES



3 LIST OF FIGURES

Functionnal description	11
STPC Host Layout	29
STPC Physical Memory Map	30
Memory Controller Interface Block Diagram	55
PCI Layout	63
South Bridge Layout	74
PRD Table Entry Example	127
Cursor Start and End Registers	183
Illustration of Page Register 0 and Page Register 1	209
GE memory Map	249
Horizontal Blanking Interval and Active Timings	339
ODDEVEN, VSYNC and HSYNC Waveforms	340
Master Mode Sync Signals	340
Memory Bank 0 Access Logic	391

LIST OF FIGURES

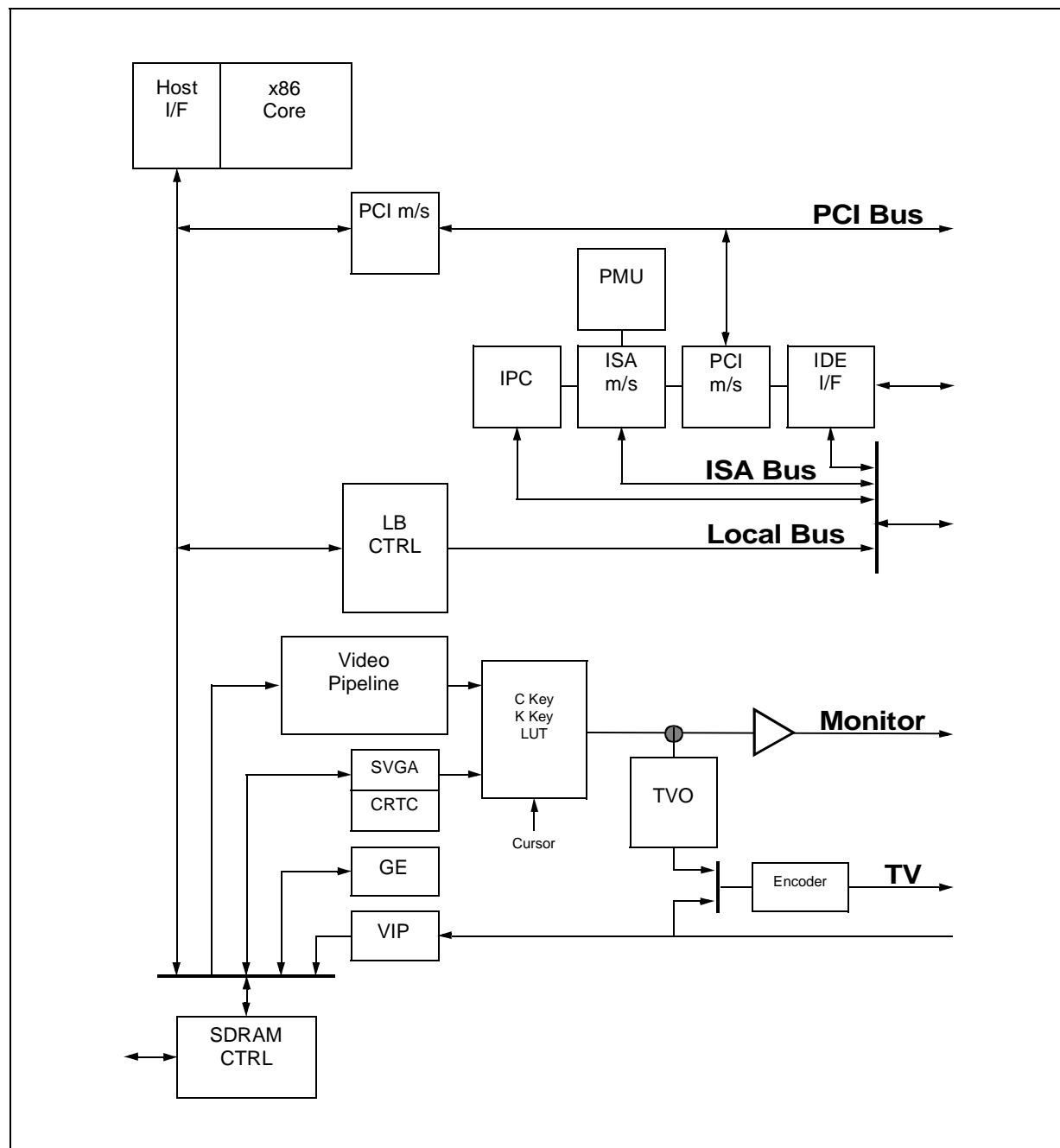
4. INTRODUCTION

This programming manual details the register sets for the STPC Consumer-II Device. The manual is split into chapters each dedicated to a function.

This document contains all the information required to program and configure the STPC Consumer-II.

In order to use this manual to the full, you may want to make reference to the STPC and X86 core Datasheets.

Figure 4-1. Functionnal description



INTRODUCTION

5. HOW TO USE THIS MANUAL

5.1. INTRODUCTION

This manual provides full technical documentation for the STPC device. It is recommended that the reader is familiar with the x86 series processors and PC compatible architectures before reading this document. Many terms are related directly to the PC architecture.

The manual itself is split into chapters. These chapters hold the information for a particular functional block of the device. For example, the chapter titled "Memory Access" gives the memory map of the STPC device, the memory architecture and interface to the external DRAM modules.

5.2. SPECIFIC NOTES

5.2.1. RESERVED BITS

Write mode 1 is a subset of Write Mode 0. No CPU-supplied write data is used. The read data latched from a previous read operation is written. The bit mask is disabled. The map-masks are implemented as they are for Write Mode 0.

Many bits in the register descriptions are noted as reserved. These bits are not internally connected, physically not present or are used for testing purposes. In all cases these bits should be set to a '0' when writing to a register with reserved bits. When reading from a register with reserved bits, these specific bits should be masked from the data value before action is taken on the data.

Any functionality found by setting the reserved bits to levels other than '0' cannot and will not be guaranteed on future revisions of the circuit design. Thus it is not recommended to use the bits marked as reserved in any way different from noted above.

5.2.2. SIGNAL ACTIVE STATE

The hash symbol (#) following a signal name indicates that when the signal is in its active (asserted) state, the signal is at a logic low level. When the "#" is not present at the end of a signal name, the logic high level represents the active state.

5.2.3. HEXADECIMAL NOTATION

In this manual Hexadecimal (Hex) numbers (numbers to the base 16: [0-9,A-F]) are denoted by the postfix 'h'.

For example a memory address 783A hexadecimal will be written 783Ah.

HOW TO USE THIS MANUAL

5.2.4. ENDIAN

In common with the x86 architecture, values in memory are little-endian, that is the lower part of the memory contains the least significant Byte.

For an 8-bit value

N	7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---	---

For a 16-bit (word) value

N	7	6	5	4	3	2	1	0
N+1	15	14	13	12	11	10	9	8

For a 24-bit value

N	7	6	5	4	3	2	1	0
N+1	15	14	13	12	11	10	9	8
N+2	23	22	21	20	19	18	17	16

For a 32-bit (long word) value

N	7	6	5	4	3	2	1	0
N+1	15	14	13	12	11	10	9	8
N+2	23	22	21	20	19	18	17	16
N+3	31	30	29	28	27	26	25	24

For a 64-bit (QUAD word) value

N	7	6	5	4	3	2	1	0
N+1	15	14	13	12	11	10	9	8
N+2	23	22	21	20	19	18	17	16
N+3	31	30	29	28	27	26	25	24
N+4	39	38	37	36	35	34	33	32
N+5	47	46	45	44	43	42	41	40
N+6	55	54	53	52	51	50	49	48
N+7	63	62	61	60	59	58	57	56

5.3. ISSUING NOTES

There are three levels identified; Advanced data, Preliminary data and Full production release.

Each level is identified in a specific way as follows.

Document Identification	Status	Definition	Release Identification
ADVANCED DATA	In design	This document based on the product specification. The information may be updated without notice. Large changes may still occur.	Release A, Release B...
PRELIMINARY DATA	Pre-production Data	This document contains preliminary data and may be updated without notice in order to improve the product features.	Issue 0.X.
FULL PRODUCTION DATA	Production Data	This is the finalised document and all test plans are completed. The information may be updated without notice in order to improve the product features.	Issue 1.X.

6 LIST OF REGISTERS

This chapter lists all the registers accessible by external software.

Section	Register Name	Mnemonic	Purpose	Address	Access type
3.	Power on strap Registers			0022h	
3.1.1	Strap register 0	Strap0	Configuration	0023h	Index 04Ah
3.1.2	Strap register 1	Strap1	Configuration		Index 04Bh
3.1.3	Strap register 2	Strap2	Configuration		Index 04Ch
3.1.4	HCLK Strap register	HCLK_Strap	Configuration		Index 05Fh
7.	Host Interface				
7.5.	Cache related registers			0022h	
7.5.1.	Cache Architecture Register 0	Cash_arc0	Configuration	0023h	Index 020h
7.5.2.	Cache Architecture Register 1	Cash_arc1	Configuration		Index 021h
7.5.3.	Cache Architecture Register 2	Cash_arc2	Configuration		Index 022h
7.6.	Address decode related registers			0022h	
7.6.1.	Memory Hole Control Register	MEM_HOLE	Configuration	0023h	Index 024h
7.6.2.	Shadow Control Register 0	SHADOW_0	Configuration		Index 025h
7.6.3.	Shadow Control Register 1	SHADOW_1	Configuration		Index 026h
7.6.4.	Shadow Control Register 2	SHADOW_2	Configuration		Index 027h
7.6.5.	Shadow Control Register 3	SHADOW_3	Configuration		Index 028h
7.6.6.	VGA Decode Register	VGA_DEC	Configuration		Index 029h
7.7.	Host SDRAM controller registers			0022h	
7.7.1.	SDRAM Bank 0 Register	SDRAM_bank0	Configuration	0023h	Index 030h
7.7.2.	SDRAM Bank 1 Register	SDRAM_bank1	Configuration		Index 031h
7.7.3.	SDRAM Bank 2 Register	SDRAM_bank2	Configuration		Index 032h
7.7.4.	SDRAM Bank 3 Register	SDRAM_bank3	Configuration		Index 033h
7.7.5.	Graphics Memory Size Register	GRAPH_MEM	Configuration		Index 036h
7.7.6.	SDRAM Refresh Register	SDRAM_Ref	Configuration		Index 039h
7.7.7.	Presents Detect Register	Pres_dect	Configuration		Index 097h
8.3.	Memory Interface			GBase+4C6000h	
8.3.1.	Register 0	MEM_REG0	Configuration		000h
8.3.2.	Register 1	MEM_REG1	Configuration		004h
8.3.3.	Register 2	MEM_REG2	Configuration		008h
8.4.	MCLK Control Registers			22h	
8.4.1.	MCLK Control Register 0	MCLK00		23h	Index 0x40h
8.4.2.	MCLK Control Register 1	MCLK01			Index 0x41h
9.5.	North Bridge Config Registers				
9.3.	Configuration Address Register	Config_address	IO	0xCF8h	

LIST OF REGISTERS

Section	Register Name	Mnemonic	Purpose	Address	Access type
9.4.	Configuration Data Register	Config_data	IO	0xCFC - CFFh	
9.5.	North Bridge Vendor Identification Register	NB_V_ID	PCI Config		Index 0x0h
9.5.	North Bridge Device Identification Register	NB_D_ID	PCI Config		Index 0x2h
9.5.1.	North Bridge PCI Command Register	NB_Com	PCI Config		Index 0x4h
9.5.2.	North Bridge PCI Status Register	NB_Stat	PCI Config		Index 0x6h
9.5.3.	North Bridge PCI Revision Id Register	NB_R_ID	PCI Config		Index 0x8h
9.5.4.	North Bridge Device Class Code Register	NB_C_Code	PCI Config		Index 0x9h
9.5.5.	North Bridge Header Type Register	NB_Hesd	PCI Config		Index 0x0Eh
9.5.6.	North Bridge Control Register	NB_Cont	PCI Config		Index 0x50h
9.5.7.	North Bridge PCI Error Status Register	NB_E_Stat	PCI Config		Index 0x54h
9.7.	South Bridge PCI Function 0 Configuration Registers			0xCF8h	
9.7.	South Bridge Vendor Identification Register	SB_V_ID0	PCI config F#0	0xCFCCh	Index 0x0h
9.7.	South Bridge Device Identification Register	SB_D_ID0	PCI Config F#0		Index 0x2h
9.7.1.	South Bridge PCI Command Register	SB_Com0	PCI Config F#0		Index 0x4h
9.7.2.	South Bridge PCI Status Register	SB_Stat0	PCI Config F#0		Index 0x6h
9.7.3.	South Bridge PCI Revision Id Register	SB_R_ID0	PCI Config F#0		Index 0x8h
9.7.4.	South Bridge Device Class Code Register	SB_C_Code0	PCI Config F#0		Index 0x9h
9.7.5.	South Bridge Header Type Register	SB_Head0	PCI Config F#0		Index 0xEh
9.7.6.	South Bridge Miscellaneous Register	SB_Misc0			Index 040h
9.8.	South Bridge PCI Function 1 Configuration Registers			0xCF8h	
7.11.1.	South Bridge Vendor Identification Register	SB_V_ID1	PCI config F#1	0xCFCCh	Index 0x0h
7.11.2.	South Bridge Device Identification Register	SB_D_ID1	PCI Config F#1		Index 0x2h
7.11.3.	South Bridge PCI Command Register	SB_Com1	PCI Config F#1		Index 0x4h
7.11.4.	South Bridge PCI Status Register	SB_Stat1	PCI Config F#1		Index 0x6h
7.11.5.	South Bridge Revision ID Register	SB_R_ID1	PCI Config F#1		Index 0x8h
7.11.5.	South Bridge Programming Interface Register	Prog_Int	PCI Config F#1		Index 0x9h
7.11.6.	South Bridge Sub-Class Code Register	Sub_Class	PCI Config F#1		Index 0xAh

LIST OF REGISTERS

Section	Register Name	Mnemonic	Purpose	Address	Access type
7.11.8.	South Bridge Base-Class code Register	Base_Class	PCI Config F#1		Index 0xBh
7.11.9.	South Bridge Latency Timer control Register	Lat_T	PCI Config F#1		Index 0xDh
7.11.10.	South Bridge Header Type Register	Head_T	PCI Config F#1		Index 0xEh
7.11.11.	South Bridge Base Address 0 Register	Base0	PCI Config F#1		Index 0x10h
7.11.12.	South Bridge Base Address 1 Register	Base1	PCI Config F#1		Index 0x14h
7.11.13.	South Bridge Base Address 2 Register	Base2	PCI Config F#1		Index 0x18h
7.11.14.	South Bridge Base Address 3 Register	Base3	PCI Config F#1		Index 0x1Ch
7.11.15.	South Bridge Base Address 4 Register	Base4	PCI Config F#1		Index 0x20h
7.11.16.	South Bridge IDE Timing Register	IDE_Timing	PCI Config F#1		see Table 7-19
7.11.17.	South Bridge Miscellaneous Register	SB_Misc1	PCI Config F#1		Index 0x48h
10.4.	ISA standard Registers				
10.4.1.	DMA 1 Controller Registers	DMA_1	IO	0000h	
10.4.1.	DMA 1 Channel 0 Base and Current Count	DMA1_CBA0	IO	0001h	
10.4.1.	DMA 1 Channel 1 Base and Current Address	DMA1_CBC0	IO	0002h	
10.4.1.	DMA 1 Channel 1 Base and Current Count	DMA1_CBA1	IO	0003h	
10.4.1.	DMA 1 Channel 2 Base and Current Address	DMA1_CBC1	IO	0004h	
10.4.1.	DMA 1 Channel 2 Base and Current Count	DMA1_CBA2	IO	0005	
10.4.1.	DMA 1 Channel 3 Base and Current Address	DMA1_CBC2	IO	0006h	
10.4.1.	DMA 1 Channel 3 Base and Current Count	DMA1_CBA3	IO	0007h	
10.4.1.	DMA 1 Read Status / Write Command Register	DMA1_RSWC	IO	0008h	
10.4.1.	DMA 1 Request Register	DMA1_RR	IO	0009h	
10.4.1.	DMA 1 Read Command / Write Single Mask Register	DMA1_RCWS M	IO	000Ah	
10.4.1.	DMA 1 Mode Register	DMA1_Mode	IO	000Bh	
10.4.1.	DMA 1 Set / Clear Byte Pointer Flip - Flop	DMA1_SCBPF F	IO	000Ch	
10.4.1.	DMA 1 Read Temp Register / Master Clear	DMA1_RTMC	IO	000Dh	
10.4.1.	DMA 1 Clear Mask / Clear All Request	DMA1_CMCA R	IO	000Eh	
10.4.1.	DMA 1 Read / Write all Mask Register Bits	DMA1_RWMB	IO	000Fh	

LIST OF REGISTERS

Section	Register Name	Mnemonic	Purpose	Address	Access type
10.4.2.	Interrupt Controller 1 Registers	IC_1	IO	0020h	
10.4.3.	Interval Timer Registers	IT_1	IO	0040h	
10.4.3.	Interval Timer Register Counter 0 Count	IT_0	IO	0040h	
10.4.3.	Interval Timer Register Counter 1 Count	IT_1	IO	0041h	
10.4.3.	Interval Timer Register Counter 2 Count	IT_2	IO	0042h	
10.4.3.	Command Mode Register	IT_3	IO	0043h	
10.4.4.	Port B Register	Port_B	IO	0061h	
10.4.5.	Port 70 Register	Port_70	IO	0070h	
10.4.6.	Interrupt Controller 2 Registers	IC_2	IO	00A0h	
10.4.7.	DMA Controller 2 Registers	DMA_Cont2	IO		
10.4.7.	DMA 2 Channel 0 Base and Current Address	DMA2_CBA0	IO	00C0h	
10.4.7.	DMA2 Channel 0 Base and Current Count	DMA2_CBC0	IO	00C2h	
10.4.7.	DMA 2 Channel 1 Base and Current Address	DMA2_CBA1	IO	00C4h	
10.4.7.	DMA 2 Channel 1 Base and Current Count	DMA2_CBC1	IO	00C6h	
10.4.7.	DMA 2 Channel 2 Base and Current Address	DMA2_CBA2	IO	00C8h	
10.4.7.	DMA 2 Channel 2 Base and Current Count	DMA2_CBC2	IO	00CAh	
10.4.7.	DMA 2 Channel 3 Base and Current Address	DMA2_CBA3	IO	00CCh	
10.4.7.	DMA 2 Channel 3 Base and Current Count	DMA2_CBC3	IO	00CEh	
10.4.7.	DMA 2 Read Status / Write Command Register	DMA2_RSWC	IO	00D0h	
10.4.7.	DMA 2 Request Register	DMA2_RR	IO	00D2h	
10.4.7.	DMA 2 Read Command / Write Single Mask Register	DMA2_RCWS M	IO	00D4h	
10.4.7.	DMA 2 Mode Register	DMA2_Mode	IO	00D6h	
10.4.7.	DMA 2 Set / Clear Byte Pointer Flip - Flop	DMA2_SCBPF F	IO	00D8h	
10.4.7.	DMA 2 Read Temporary / Master Clear	DMA2_RTMC	IO	00DAh	
10.4.7.	DMA 2 Clear Mask / Clear All Requests Register	DMA2_CMCA R	IO	00DCh	
10.4.7.	DMA 2 Read / Write all Mask Register Bits	DMA2_RWMR B	IO	00DEh	
10.4.8.	DMA Page Registers	DMA_Page	IO		
10.4.8.	DMA Page Registers Port 80h (reserved)	Port_80	IO	0080h	
10.4.8.	DMA Page Register Channel 2	DMA_PRC2	IO	0081h	
10.4.8.	DMA Page Register Channel 3	DMA_PRC3	IO	0082h	
10.4.8.	DMA Page Register Channel 1	DMA_PRC1	IO	0082h	
10.4.8.	DMA Page Register Port 84h	Port_84	IO	0084h	(Reserved)

LIST OF REGISTERS

Section	Register Name	Mnemonic	Purpose	Address	Access type
10.4.8.	DMA Page Register Port 85h	Port_85	IO	0085h	(Reserved)
10.4.8.	DMA Page Register Port 86h	Port_86	IO	0086h	(Reserved)
10.4.8.	DMA Page Register Channel 0	DMA_PRC0	IO	0087h	
10.4.8.	DMA Page Register Port 87h	Port_87	IO	0088h	
10.4.8.	DMA Page Register Channel 6	DMA_PRC6	IO	0089h	
10.4.8.	DMA Page Register Channel 7	DMA_PRC7	IO	008Ah	
10.4.8.	DMA Page Register Channel 5	DMA_PRC5	IO	008Bh	
10.4.8.	DMA Page Register Port 8Bh	Port_8B	IO	008Ch	(Reserved)
10.4.8.	DMA Page Register Port 8Ch	Port_8C	IO	008Dh	(Reserved)
10.4.8.	DMA Page Register Port 8Dh	Port_8D	IO	008Eh	(Reserved)
10.4.8.	DMA Page Register Port 8Eh	Port_8E	IO	008Fh	(Reserved)
10.5.	ISA Configuration Registers			0022h	
10.5.1.	Miscellaneous Control Register 0	Misc_Cont0	Configuration	0023h	Index 050h
10.5.2.	Miscellaneous Control Register 1	Misc_Cont1	Configuration		Index 051h
10.5.3.	PIRQA Routing control Register 0	PAR_Cont0	Configuration		Index 052h
10.5.3.	PIRQB Routing control Register 0	PBR_Cont0	Configuration		Index 053h
10.5.3.	PIRQC Routing control Register 0	PCR_Cont0	Configuration		Index 054h
10.5.3.	PIRQD Routing control Register 0	PDR_Cont0	Configuration		Index 055h
10.5.4.	Interrupt Level Control Register 0	IRQ_Lev_C_0	Configuration		Index 056h
10.5.5.	Interrupt Level Control Register 1	IRQ_Lev_C_1	Configuration		Index 057h
10.5.6.	IPC Configuration Register	IPC_Conf	Configuration		Index 001h
10.5.7.	VMI IRQ Routing Control Register	VIR_Cont	Configuration		Index 058h
10.5.8.	ISA Synchronizer Bypass Register	ISA_Sync	Configuration		Index 059h
12.3.	VGA registers				
12.4.	General Registers				
12.4.1.	Motherboard Enable Register	MBEN		0x094h	
12.4.2.	Add-in VGA Enable Register	ADDEN		0x46E8h	
12.4.3.	Video Subsystem Enable 1 Register	VSE1		0x102h	
12.4.4.	Video Subsystem Enable 2 Register	VSE2		0x3C3h	
12.4.5.	Miscellaneous Output Register	MISC		0x3CC/ 0x3C2h	
12.4.6.	Input Status Register #0	INP0		0x3C2h	
12.4.7.	Input Status Register #1	INP1		0x3XAh	
12.5.	Sequencer Registers				
12.5.1.	Sequencer Index Register	SRX		0x03C4h	
12.5.2.	Sequencer Reset Register	SR0		0x03C5h	Index 000h
12.5.3.	Sequencer Clocking Mode Register	SR1			Index 001h
12.5.4.	Sequencer Plane Mask Register	SR2			Index 002h
12.5.5.	Sequencer Character Map Register	SR3			Index 003h
12.5.6.	Sequencer Memory Mode Register	SR4			Index 004h
12.5.7.	Extended Register Lock/Unlock Register	SR6			Index 006h

LIST OF REGISTERS

Section	Register Name	Mnemonic	Purpose	Address	Access type
12.6.	Graphics Controller Registers				
12.6.1.	Graphics Controller Index Register	GRX		0x03CEh	
12.6.2.	Graphics Set/Reset Register	GR0		0x03CFh	Index 000h
12.6.3.	Graphics Enable Set/Reset Register	GR1			Index 001h
12.6.4.	Graphics Color Compare Register	GR2			Index 002h
12.6.5.	Raster Op/Rotate Count Register	GR3			Index 003h
12.6.6.	Graphics Read Map Select Register	GR4			Index 004h
12.6.7.	Graphics Mode Register	GR5			Index 005h
12.6.8.	Graphics Miscellaneous Register	GR6			Index 006h
12.6.9.	Graphics Color Don't Care Register	GR7			Index 007h
12.6.10.	Graphics Bit Mask Register	GR8			Index 008h
12.7.	Attribute Controller Registers				
12.7.1.	Attribute Controller Index Register	ARX		0x3C0h	
12.7.2.	Attribute Palette Registers	AR0 - ARF		0x3C1/ 0x3C0h	
12.7.3.	Attribute Ctrl Mode Register	AR10		0x3C1/ 0x3C0h	
12.7.4.	Attribute Ctrl Overscan Color Register	AR11		0x3C1/ 0x3C0h	
12.7.5.	Attribute Color Plane Enable Register	AR12		0x3C1/ 0x3C0h	
12.7.6.	Attribute Horz Pixel Panning Register	AR13		0x3C1/ 0x3C0h	
12.7.7.	Attribute Color Select Register	AR14		0x3C1/ 0x3C0h	
12.8.	CRT Controller Registers				
12.8.1.	Index Register	CRX	see Note 1	0x3X4h	
12.8.2.	Horizontal Total Register	CR0	see Note 1	0x3X5h	Index 000h
12.8.3.	Horiz display End Register	CR1			Index 001h
12.8.4.	Horiz Blanking Start Register	CR2			Index 002h
12.8.5.	Horiz Blanking End Register	CR3			Index 003h
12.8.6.	Horiz Retrace Start Register	CR4			Index 004h
12.8.7.	Horizontal Retrace end Register	CR5			Index 005h
12.8.8.	Vertical Total Register	CR6			Index 006h
12.8.9.	Overflow Register	CR7			Index 007h
12.8.10.	Screen A Preset Row Scan Register	CR8			Index 008h
12.8.11.	Character Cell Height Register	CR9			Index 009h
12.8.12.	Cursor Start Register	CRA			Index 00Ah
12.8.13.	Cursor End Register	CRB			Index 00Bh
12.8.14.	Start Address High Register	CRC			Index 00Ch
12.8.15.	Start Address Low Register	CRD			Index 00Dh
12.8.16.	Text Cursor Offset High Register	CRE			Index 00Eh
12.8.17.	Text Cursor Offset Low Register	CRF			Index 00Fh
12.8.18.	Vertical Retrace Start Register	CR10			Index 010h
12.8.19.	Vertical Retrace End Register	CR11			Index 011h

LIST OF REGISTERS

Section	Register Name	Mnemonic	Purpose	Address	Access type
12.8.20.	Vertical Display End Register	CR12			Index 012h
12.8.21.	Offset Register	CR13			Index 013h
12.8.22.	Underline Location Register	CR14			Index 014h
12.8.23.	Vertical Blanking Start reg	CR15			Index 015h
12.8.24.	Vertical Blanking End Register	CR16			Index 016h
12.8.25.	Mode Register	CR17			Index 017h
12.8.26.	Line Compare Register	CR18			Index 018h
12.8.27.	Graphics Control Data	CR22			Index 019h
12.8.28.	Attribute Address Flipflop	CR24			Index 020h
12.8.29.	Attribute Index Readback	CR26			Index 021h
12.9.	VGA Extended Registers		<i>see Note 1</i>	0x3X4h	
12.9.1.	Repaint Control Register 0	CR19	<i>see Note 1</i>	0x3X5h	Index 019h
12.9.2.	Repaint Control Register 1	CR1A			Index 01Ah
12.9.3.	Repaint Control Register 2	CR1B			Index 01Bh
12.9.4.	Repaint Control Register 3	CR1C			Index 01Ch
12.9.5.	Page Register 0	CR1D			Index 01Dh
12.9.6.	Page Register 1	CR1E			Index 01Eh
12.9.7.	Graphics Extended Enable Register	CR1F			Index 01Fh
12.9.8.	Graphics Extended GBASE Register	CR20			Index 020h
12.9.9.	Graphics Extended Aperture Register	CR21			Index 021h
12.9.10.	Repaint Control Register 4	CR25			Index 025h
12.9.11.	Repaint Control Register 5	CR27			Index 027h
12.9.12.	Palette Control Register	CR28			Index 028h
12.9.13.	Cursor Height Register	CR29			Index 029h
12.9.14.	Cursor Color 0 Register A	CR2A			Index 02Ah
12.9.15.	Cursor Color 0 Register B	CR2B			Index 02Bh
12.9.16.	Cursor Color 0 Register C	CR2C			Index 02Ch
12.9.17.	Cursor Color 1 Register A	CR2D			Index 02Dh
12.9.18.	Cursor Color 1 Register B	CR2E			Index 02Eh
12.9.19.	Cursor Color 1 Register C	CR2F			Index 02Fh
12.9.20.	Graphics Cursor Address Register 0	CR30			Index 030h
12.9.21.	Graphics Cursor Address Register 1	CR31			Index 031h
12.9.22.	Graphics Cursor Address Register 2	CR32			Index 032h
12.9.23.	Urgent Start Register	CR33			Index 033h
12.9.24.	Displayed Frame Y Offset 0 Register	CR34			Index 034h
12.9.25.	Displayed Frame Y Offset 1 Register	CR35			Index 035h
12.9.26.	Interlace Half Field Start Register	CR39			Index 039h
12.9.26.	Implementation Number Register	CR3A			Index 03Ah
12.9.28.	Graphics Version Register	CR3B			Index 03Bh
12.9.29.	Miscellaneous Test Register	CR3E			Index 03Eh
12.9.30.	DDC Control Register	CR3F			Index 03Fh

LIST OF REGISTERS

Section	Register Name	Mnemonic	Purpose	Address	Access type
12.9.31.	TV Interface Control Register	CR40			Index 040h
12.9.32.	TV Horizontal Active Video Start A Register	CR41			Index 041h
12.9.33.	TV Horizontal Active Video Start B Register	CR42			Index 042h
12.9.34.	TV Horizontal Sync End A Register	CR43			Index 043h
12.9.35.	TV Horizontal Sync End B Register	CR44			Index 044h
12.12.	RAMDAC registers				
12.12.1.	Palette Pixel Mask Register	Pixel_Mask		0x3C6h	
12.12.2.	Palette Read index Register	Read_index		0x3C7h	
12.12.3.	Palette State Register	Palette_State		0x3C7h	
12.12.4.	Palette Write Index Register	Write_index		0x3C8h	
12.12.5.	Palette Data Register	Palette_data		0x3C9h	
12.13	DCLK Control Registers			22h	
12.13.1.	DCLK Control Register 00	DCLK00	PCI Config	23h	Index 0x42h
12.13.2.	DCLK Control Register 01	DCLK01	PCI Config		Index 0x43h
12.13.3.	DCLK Control Register 10	DCKL10	PCI Config		Index 0x44h
12.13.4.	DCLK Control Register 11	DCLK11	PCI Config		Index 0x45h
12.13.5.	DCLK Control Register 20	DCLK20	PCI Config		Index 0x46h
12.13.6.	DCLK Control Register 21	DCLK21	PCI Config		Index 0x47h
12.13.7.	DCLK Control Register 30	DCLK30	PCI Config		Index 0x48h
12.13.8.	DCLK Control Register 31	DCLK31	PCI Config		Index 0x49h
13.5.	VGA Operand Source				
13.9.1.	Back Ground Color Register	Background		8400000h	Index 0x004h
13.9.2.	Cursor Coordinate Register	Cursor_XY			Index 0x11Ch
13.9.3.	Top of Data FIFO Register	Data_Port			Index 0x804h
13.9.4.	Destination Operand Base Address Register	Dst_base			Index 0x018h
13.9.5.	Destination Pitch Register	Dst_pitch			Index 0x028h
13.9.6.	Destination Operand Coordinate Register	Dst_XY		8410000h	
13.9.7.	Foreground Color Register	Foreground		8400000h	Index 0x034h
13.9.8.	Height Register	Height			Index 0x048h
13.9.9.	Pattern Base Address Operand Register	Pattern			Index 0x058h
13.9.10.	Pixel Depth Operand Register	Pixel_depth			Index 0x07Ch
13.9.11.	Raster Operation Register	ROP			Index 0x08Ch
13.9.12.	Source Base Address Operand Register	Src_base			Index 0x098h
13.9.13.	Source Pitch Operand Register	Src_pitch			Index 0x0ACh
13.9.14.	Source Coordinate Register	Src_XY			Index 0x0BDh
13.9.15.	Status Register	Status			Index 0x908
13.9.16.	Width Register	Width			Index 0x0C8h
13.9.17.	Extra Use Register	Xtra			Index 0x0D4h
13.9.18.	SRC Transparency Compare Register	SRC_transparency			Index 0xECh

LIST OF REGISTERS

Section	Register Name	Mnemonic	Purpose	Address	Access type
13.9.19.	DST Transparency Compare Register	DST_transparency			Index 0xFC
14.6.	Video Input Port Registers				
14.6.1.	Frame Buffer Address Readback Register	FB1_adr		GBase +600000h	Index 0x00h
14.6.2.	Video Input Port Configuration Register	Vin_CFG			Index 0x04h
14.6.3.	Video Input Port Status Register	Vin_stat			Index 0x08h
14.6.4.	Video Input Buffer Addr 0	Vin_ad0			Index 0x0Ch
14.6.5.	Video Input Buffer Addr 1	Vin_ad1			Index 0x10h
14.6.6.	Video Input Desination Pitch	Vin_dp			Index 0x14h
14.6.7.	External Timing Generator 1	Vtg_ext1			Index 0x28h
14.6.8.	External Timing Generator 2	Vtg_ext2			Index 0x2Ch
14.6.9.	Horizontal Timing Generator	Vtg_ht			Index 0x30h
14.6.10.	Video Timing Generator	Vtg_vf			Index 0x34h
14.6.11.	Limit Address Register	Laddr0			Index 0x3Ch
16.6.	Video Output Port Register			GBase+4CA000h	
16.6.1.	Register_0.Configuration0	Config0			Index 000h
16.6.2.	Register_1.Configuration1	Config1			Index 001h
16.6.3.	Register_2.Configuration2	Config2			Index 002h
16.6.4.	Register_3.Configuration3	Config3			Index 003h
16.6.5.	Register_4.Configuration4	Config4			Index 004h
16.6.6.	Register_5.Configuration5	Config5			Index 005h
16.6.7.	Register_6.Configuration6	Config6			Index 006h
16.6.9.	Register_8.Status	Stat8			Index 008h
16.6.10.	Register_9.Status	Stat9			Index 009h
16.6.11.	Register_10.Increment_dfs	Incr_10			Index 010h
16.6.11.	Register_11.Increment_dfs	Incr_11			Index 011h
16.6.11.	Register_12.Increment_dfs	Incr_12			Index 012h
16.6.12.	Register_13.Phase_dfs	Phase_13			Index 013h
16.6.12.	Register_14.Phase_dfs	Phase_14			Index 014h
16.6.19.	Register_21:line_reg=ltarg[8:1]	Reg_21			Index 021h
16.6.19.	Register_22:line_reg=ltarg[0] and lref[8:2]	Reg_22			Index 022h
16.6.20.	Register_23:line_reg=ltarg[1:0]	Reg_23			Index 023h
16.6.20.	Register_31.cgms_bit [1:4]	Reg31			Index 031h
16.6.20.	Register_32.cgms_bit [5:12]	Reg32			Index 032h
16.6.20.	Register_33.cgms_bit [13:20]	Reg33			Index 033h
16.6.26.	Register_39.cccf1	Reg39			Index 039h
16.6.26.	Register_40.cccf1	Reg40			Index 040h
16.6.27.	Register_41.cccf2	Reg41			Index 041h
16.6.27.	Register_42.cccf2	Reg42			Index 042h
16.6.28.	Register_43.cclif1	Reg43			Index 043h
15.	Video Pipeline Registers				
15.3.	Source Specification Registers		see Note 2	X600000h	
15.3.1.	Video Source Base Register	Video_Src_Base			Index 0x0h

LIST OF REGISTERS

Section	Register Name	Mnemonic	Purpose	Address	Access type
15.3.2.	Video Source Pitch Register	Video_Src_Pitch			Index 0x4h
15.3.3.	Video Source Dimension Register	Vid_Src_dim			Index 0x8h
15.3.4.	CRTC Burst Length Register	CRTC_Burst_Length			Index 0xCh
15.3.5.	Video Burst Length Register	Vid_Burst_Length			Index 0x10h
15.4.	Destination Specification Registers				
15.4.1.	Video Destination Register	Vid_Dst_XY			Index 0x14h
15.4.2.	Video Destination Dimension Register	Vid_Dst_dim			Index 0x18h
15.5.	Filter Control Register				
15.5.1.	Horizontal Scaling and Decimation Register	Horiz_Scale			Index 0x20h
15.5.2.	Vertical Control and Decimation Register	Vert_Scale			Index 0x28h
15.5.3.	Color Space Converter Specification Register	Color_Con_Spec			Index 0x2Ch
15.6.	Video and Graphics mixing control Registers				
15.6.1.	Mix Mode Register	Mix_Mode			Index 0x30h
15.6.2.	Color Key Register	CCLR_Key			Index 0x34h
15.6.3.	Chroma Key Low Register	CKL			Index 0x38h
15.6.4.	Chroma Key High Register	CKH			Index 0x3Ch
15.6.5.	Status Register	Filter_Stat			Index 0x40h
17.2.	Local Bus Registers		16 bit access	22h	
17.3.	Local Bus Address Decode Registers			23h	
17.3.1.	I/O Slot Base Register 0	IOAREG0			Index 0x10h
17.3.2.	I/O Slot Base Register 1	IOAREG1			Index 0x11h
17.3.3.	I/O Slot Base Register 2	IOAREG2			Index 0x12h
17.3.4.	I/O Slot Base Register 3	IOAREG3			Index 0x13h
17.3.5.	I/O Slot Mask Register 0	IOMREG0			Index 0x14h
17.3.6.	I/O Slot Mask Register 1	IOMREG1			Index 0x15h
17.4.	Local Bus Timing Registers				
17.4.1.	Memory Timing Template 0	TIMEBANK0			Index 0x16h
17.4.2.	Memory Timing Template 1	TIMEBANK1			Index 0x17h
17.4.3.	I/O Timing Template 0	TIMEIO0			Index 0x18h
17.4.4.	I/O Timing Template 1	TIMEIO1			Index 0x19h
17.4.5.	I/O Timing Template 2	TIMEIO2			Index 0x1Ah
17.4.6.	I/O Timing Template 3	TIMEIO3			Index 0x1Bh
17.5.1.	Local Bus Control Register				
17.5.1.	Control Register	CONTROL			Index 0x1Ch
17.5.2.	I/O Width Register	IOWIDTH			Index 0x1Eh

LIST OF REGISTERS

Section	Register Name	Mnemonic	Purpose	Address	Access type
18.2.	Power Management Controller Registers:			0022h	
18.2.1.	Timer Register 0	Timer0	Configuration	0023h	Index 060h
18.2.2.	Timer Register 1	Timer1	Configuration		Index 061h
18.2.3.	Timer Register 2	Timer2	Configuration		Index 08dh
18.2.4.	System Activity Enable Register 0	Sys_activ_en0	Configuration		Index 062h
18.2.5.	System Activity Enable Register 1	Sys_activ_en1	Configuration		Index 063h
18.2.6.	System Activity Enable Register 2	Sys_activ_en2	Configuration		Index 064h
18.2.7.	House-Keeping Activity Enable Register 0	HK_activ_en0	Configuration		Index 065h
18.2.8.	House-Keeping Activity Enable Register 1	HK_activ_en1	Configuration		Index 066h
18.2.9.	Peripheral Inactivity Detection Register 0	Perif_inactiv0	Configuration		Index 067h
18.2.10.	Peripheral Activity Detection Register 0	Perif_activ0	Configuration		Index 069h
18.2.11.	Peripheral Activity Detection Register 1	Perif_activ1	Configuration		Index 06Ah
18.2.12.	Address Range 0 Register 0	Add_range0-0	Configuration		Index 06Bh
18.2.13.	Address Range 0 Register 1	Add_range0-1	Configuration		Index 06Ch
18.2.14.	SMI Control Register 0	SMI_cont0	Configuration		Index 071h
18.2.15.	SMI Status Register 0	SMI_stat0	Configuration		Index 073h
18.2.16.	SMI Status Register 1	SMI_stat1	Configuration		Index 074h
18.2.17.	Peripheral Inactivity Status Register 0	Perif_stat0	Configuration		Index 075h
18.2.18.	Activity Status Register 0	Activ_stat0	Configuration		Index 077h
18.2.19.	Activity Status Register 1	Activ_stat1	Configuration		Index 078h
18.2.20.	Activity Status Register 2	Activ_stat2	Configuration		Index 079h
18.2.21.	PMU State Register	PMU	Configuration		Index 07Ah
18.2.22.	General Purpose Register	GP	Configuration		Index 07Bh
18.2.23.	Clock Control Register 0	Clock_cont0	Configuration		Index 07Ch
18.2.24.	Doze Timer Read Back Register	Doze	Configuration		Index 088h
18.2.25.	Standby Timer Read Back Register	Standby	Configuration		Index 089h
18.2.26.	Suspend Timer Read Back Register	Suspend	Configuration		Index 08Ah
18.2.27.	House-Keeping Timer Read Back Register	HK_timer	Configuration		Index 08Bh
18.2.28.	Peripheral Timer Read Back Register	Perif_timer	Configuration		Index 08Ch

Note 1: X can stand for B (Monochrome Display) or D (Color Display)

Note 2: X is the value of the G_Base and can range from 8h to Fh.

LIST OF REGISTERS

Table 6-1. CPU Registers located in the ST 486 Programming Manual

Register Name	Mnemonic	Purpose	Address	Access type
Configuration Registers			22h	
Configuration Control 1	CCR1	IO	23h	C1h
Configuration Control 2	CCR2	IO		C2h
Configuration Control 3	CCR3	IO		C3h
SMM Address Region	SMAR	IO		CDH
Device Identification 0	DIR0	IO		FEh
Device Identification 1	DIR1	IO		FFh

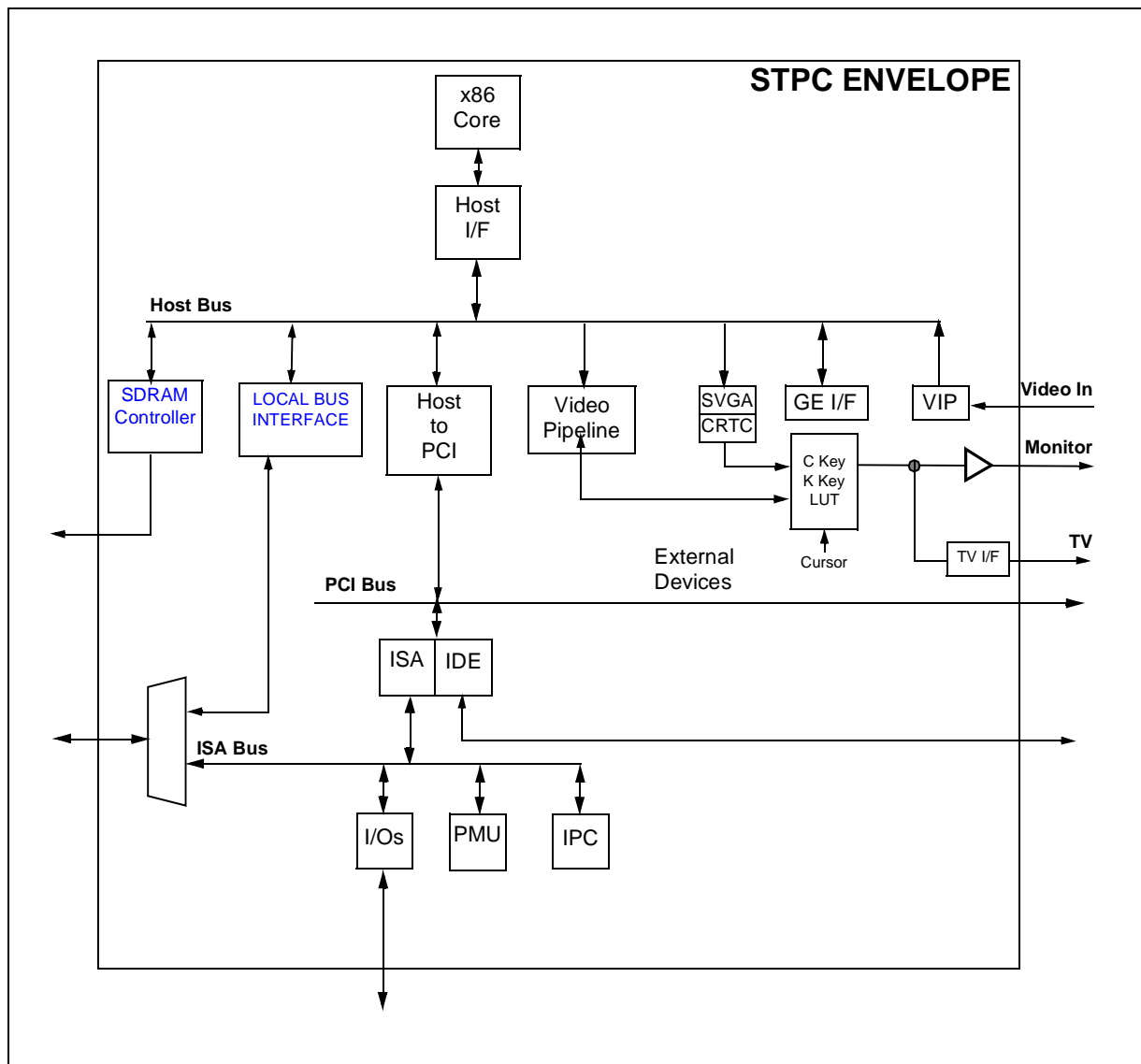
7. HOST INTERFACE

7.1. INTRODUCTION

This Chapter describes the Memory and I/O Mapping of the STPC with details on how to configure the Cache Memory registers.

The Host is the main interface between the CPU and the other integrated peripherals of the STPC. [Figure 7-1](#) below illustrates the relation of the integrated devices with reference to the Host Interface.

Figure 7-1. STPC Host Layout



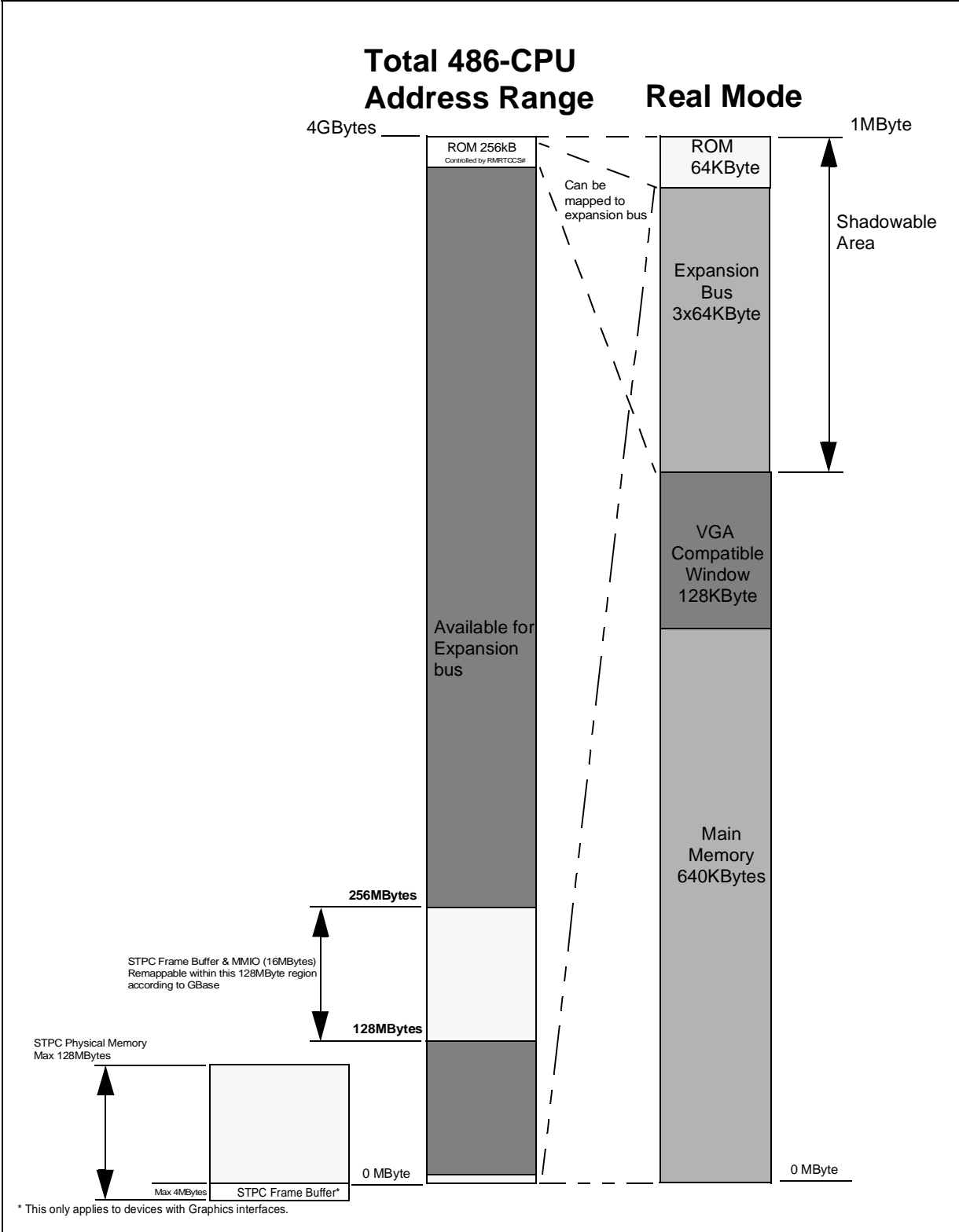


Figure 7-2. STPC Physical Memory Map

7.2. AGENT DECODING

All agents are decoded on a priority basis for instructions that are sent from the Host onto the host bus. If no agent on the Host Bus claims the cycle, it is then taken by the Host to PCI bridge (PCI North Bridge). If no agent on the PCI bridge claims the cycle it is forwarded to the ISA bridge.

For PCI Memory accesses, the cycle is forwarded to the Host Bridge to be decoded in by the SDRAM Controller. PCI Master cycles follow the procedure above. For ISA Master devices, the cycle is first forwarded to the PCI Bridge and follows the procedure described above. ISA Memory cycles are forwarded in the same way as the PCI Memory cycles.

7.3. MEMORY ADDRESS MAP

Figure 7-2 illustrate the STPC Memory Map including the general overview of how the SDRAM controller is situated within the complete map including the STPC Frame Buffer Location.

Memory Region	Address Range	Description
MAIN MEMORY (640K)	00000000h 0009FFFFh	Host access maps to the main memory and no ISA or PCI cycle will be initiated. PCI master cycles in this range maps to main memory provided they are not claimed by a PCI Slave. The STPC relies on subtractive decode before initiating an internal memory cycle. ISA master cycles in this range maps to main memory. The STPC will negate IOCHRDY if necessary. The DMA master cycles in this range maps to main memory. The STPC will actively drive the SD bus during target reads and modify main memory for target write transfers. This address segment is considered always cacheable in the L1 cache. PCI and ISA master cycles in this range, require the L1 cache.
VGA FRAME BUFFER (128K)	000A0000h 000BFFFFh	This 128K address segment contains the VGA Frame buffer. Normally this address segment is mapped to the DOS frame buffer located in the main memory. However, if VGA is disabled or the VGA memory map mode is such that the VGA does not occupy the entire 128K address range, the host cycle is forwarded to the PCI bus and if not claimed by a PCI slave, it is further forwarded to the ISA bus. The PCI master cycles in this range, if not claimed by a PCI slave, will be mapped to the main memory or will be forwarded to the ISA bus as per the VGA decode described above. Similarly, the ISA or DMA master cycles will either map to the main memory or will be forwarded to the PCI. If no PCI slave claims the cycle, the STPC assumes existence of an ISA memory device at this address range. This segment is never cacheable.
SHADOW (16K)	000C0000h 000C3FFFh	This 16K address segment can be programmed software to either map to main memory or expansion buses. Further, reads and writes can have different mappings. If mapped to main memory, this segment will behave as the 0-640K segment. If not mapped to main memory, refer to Section 7.2. above If mapped to the main memory, the cacheability of this address range is controlled by software. If mapped to the ISA bus, the ROMCS# signal may optionally be asserted as controlled by software. This allows the system and video/peripheral BIOS to physically reside in a single ROM device.

HOST INTERFACE

Memory Region	Address Range	Description
SHADOW (16K)	000C4000h 000C7FFFh	This range has the same characteristics as that of 000C0000h-000C3FFFh segment, as described above. The shadow control for this address range is provided via Shadow Control register 0 and cacheability and ROM chip-select control via Shadow Control register 3.
SHADOW (16K)	000C8000h 000CBFFFh	This range has the same characteristics as that of 000C0000h-000C3FFFh segment as described above, with the exception of the cacheability attribute. This address range is hardwired to be non-cacheable. Shadow control for this address range is provided via Shadow Control register 0 and ROM chip-select control via Shadow Control register 3.
SHADOW (16K)	000CC000h 000CFFFFh	This range has the same characteristics as that of 000C8000h-000CBFFFh segment, as described above. Shadow control for this address range is provided via Shadow Control register 0 and ROM chip-select control via Shadow Control register 3. This address range is hardwired to be non-cacheable.
SHADOW (64K)	000D0000h 000DFFFFh	This range has the same characteristics as that of 000CC000h-000CFFFFh segment, as described above. Shadow control for this address range is provided via Shadow Control register 1 and can be controlled at 16K resolution. ROM chip-select generation for the entire 64K range can be controlled via Shadow Control register 3. This address range is hardwired to be non-cacheable.
SHADOW (64K)	000E0000h 000EFFFFh	This range has the same characteristics as that of 000CC000h-000CFFFFh segment, as described above. Shadow control for this address range is provided via Shadow Control register 2 and can be controlled at 16K resolution. ROM chip-select generation for the entire 64K range can be controlled via Shadow Control register 3. This address range is hardwired to be non-cacheable.
SHADOW (64K)	000F0000h 000FFFFFFh	This range has the same characteristics as that of 000C0000h-000C7FFFh segment, as described above. Shadow control for this address range is provided via Shadow Control register 3. If not shadowed in the main memory, cycles in this address range which are forwarded to the ISA bus will always results in an ROMCS# assertion. The cacheability of this address segment is controlled via Shadow Control register 3.
TOP OF ADDRESSABLE SDRAM MEMORY (1M)	00100000h	This address segment is mapped to the main memory with the exception of one hole that can optionally be opened in the range 1MBytes to 16 Mytes. The address range defined for the hole is mapped to the expansion buses and is described later in this section. The addressable SDRAM memory can be different from the populated memory due to the memory remapping and the frame buffer. This is described in more detail in a later section. With the exception of the memory holes, this address range has the same characteristics as the 0-640K (compatible DOS memory) range.
TOP OF ADDRESSABLE SDRAM MEMORY (4G-256K)	FFFC0000h	All cycles above the addressable SDRAM memory are forwarded to the expansion buses. Host access in this range initiates a PCI cycle and if unclaimed by a PCI slave, they are forwarded to ISA. Note that the ISA address space is only 16M. Higher addresses are aliased to this 16M space.
ROM ALIAS (4G-64K)	FFFF0000 FFFFFFFFh	This address segment is an alias of the 64K segment located at F0000h-FFFFFFh and has the same attributes except that this segment can never be shadowed into the SDRAM memory. This is also true for address E0000h, D0000h and C0000h provided I/O register Index 51h (see Section 9.13.2.) is set correctly.

7.3.1. EXTENDED GRAPHICS SEGMENT

A 16M segment of memory anywhere between Top of addressable SDRAM memory and 256M can be optionally enabled via extended VGA Graphics Registers (GRA). This segment is located at 16M granularity. Refer to the Graphics section for a more detailed description of the layout of this memory segment.

Host access to this region is absorbed by the STPC and are either consumed internally, or initiate a frame buffer memory access.

PCI master access to this region, if not claimed by a PCI slave is absorbed by the STPC and treated the same way as a host access.

This address range by definition is not accessible to ISA and DMA masters, since it must be located at a 16M granularity above the addressable SDRAM memory. The ISA and DMA masters can access only up to 16M address range.

This address segment is always considered non-cacheable.

7.3.2. MEMORY HOLE

The Memory Hole register allows the creation of a hole in the memory space in 1-16M address range. This hole allows mapping expansion bus cards in the AT compatible address range when the addressable main memory size exceeds 16M. A host/PCI/ISA/DMA master cycle in this address range is handled in the same way as a cycle above the addressable memory range described above.

7.3.3. SMM MEMORY

The STPC uses the physical memory behind the CPU address range A0000h - B0000h for the SMM memory. The SMM base address register inside CPU needs to be programmed to A0000h. The initialization of the SMM memory is controlled by RAM System management register and redirects the CPU A0000h-B0000h address range to SMM memory. After the initialization, SMM memory can only be accessed when SMI \overline{ACT} # is active. The cacheability of this segment is hardwired to 0.

7.3.4. ADDRESSABLE SDRAM MEMORY

Addressable SDRAM memory is a function of the size of populated SDRAM, the size of graphic memory, the size of memory hole, and the shadow control of D0000h-DFFFFh and E0000h-EFFFFh segments.

TOPM = The size of total physical SDRAM is defined by SDRAM Bank 3 Register.

TOGM = The size of graphic memory is defined by Graphic memory size register.

MHOLE_SIZE = The size of memory hole defined by Memory Hole Control register.

REMAP_SIZE = 128KB, if none of the 8 x 16KB-segments of D0000h-EFFFFh is enabled for shadow, or 0KB, if any of the 8 x 16KB-segments of D0000h-EFFFFh is enabled for shadow.

The addressable SDRAM memory =

TOPM - TOGM + MHOLE_SIZE + REMAP_SIZE

7.3.5. CPU ADDRESS TO SDRAM ADDRESS MAPPING

The STPC implements a single memory subsystem for both the system as well as the frame buffer memory. In other words, the size of the SDRAM available to the system is reduced by the size of the SDRAM allocated to the frame buffer.

The CPU's concept of a physical address is a logical address to the STPC and is remapped to a SDRAM physical address. This section refers to the CPU's physical address as the "CPU address" and to the SDRAM's physical address as the "SDRAM address".

HOST INTERFACE

The lower range of the SDRAM, starting from the SDRAM address 00h, is allocated to frame buffer. The rest of the memory is used by the system. The CPU address is mapped to the SDRAM address space above the frame buffer address space. Since the size of the frame buffer can vary and is controlled by the Graphics Memory Size Register (Index 36 of the STPC configuration registers).

STPC also defines a memory hole to allow the existence of memory devices on the PCI or ISA buses. The size of the CPU address space is increased by these memory holes, if they exist. CPU address space D0000h to EFFFFh is mapped to the add-in card BIOS area. If this ROM space is not shadowed, then the CPU address space is increased by another 128 KBytes (also see [Section 7.6.1.](#)).

For example:

Total populated SDRAM = 4 MBytes

Frame buffer size = 256 KBytes*

Memory hole size = 1 MByte

Memory hole starting address = 200000h

Shadow feature for D0000h to EFFFFh = disabled

The total CPU memory = 4 MBytes - 256 KBytes + 1 MByte + 128 KBytes = 4 MBytes plus 896 KBytes

Since the frame buffer is 256 KBytes*, the system memory is reduced by 256 KBytes and becomes 3 MBytes plus 768 KBytes. Since a 1 MByte memory hole exists, the CPU address space is increased by 1 MByte and becomes 4 MBytes plus 768 KBytes. The CPU address between 3 MBytes plus 768 KBytes and 128 MBytes above this is mapped to the memory hole.

Since the shadowing of the CPU address range D0000h to EFFFFh reserved for add-on card BIOS is not enabled, the CPU memory is increased by 128 KBytes to make use of this SDRAM space that no device accesses. The total CPU memory then becomes 4 MBytes plus 896 KBytes.

* Not applicable to STPC Elite or Vega.

7.4. IO ADDRESS MAP

Table 7-1. : IO Map Space

IO address	Description	Notes
0000h-000Fh	8237 DMA controller 1 registers.	1
0020h-0021h	8259 Interrupt controller 1 registers.	
0022h	STPC specific configuration registers index port	
0023h	STPC specific configuration registers data port	
0040h-0043h	8254 Timer/Counter registers.	1
0060h-0064h	Keyboard shadow registers.	1
0070h-0071h	NMI Mask control registers.	1
0080h-008Fh	DMA Page registers.	
0094h	Mother-board VGA enable.	2
00A0h-00A1h	8259 Interrupt controller 2 registers.	1
061h	ISA standard Port B.	1
00C0h-00DFh	8237 DMA controller 2 registers.	1
0102h	VGA setup register.	
03B4h,03B5h,03BAh	VGA registers.	
03D4h,03D5h,03DAh		
03C0h-03CFh		
0CF8h	PCI configuration Address register.	
0CFCh-0CFFh	PCI configuration Data register.	
46E8h	VGA add-in mode enable register.	2

The STPC implements a number of registers in IO address space. This is visible in the registers with access = 0022h/0023h. These registers use the index and data programming system where the index to which the data is to be written to is programmed in register 0022h and the data is written to register 0023h.

These register occupy the map in the IO space in the table above: [Table 7-1](#)

Notes:

1. This address range is partially decoded. Refer to the Register Description section for more details.
2. This address is occupied only if the STPC is strapped to look like a mother-board VGA.

7.4.1. PCI CONFIGURATION ADDRESS MAP:

The STPC occupies Device number 0 slot on the PCI bus and implements a number of registers in PCI configuration address space. These registers occupy the following map (see [Table 7-2](#)) :

Table 7-2. PCI Configuration Address Space

Offset	Description
00h-01h	Vendor Identification register
02h-03h	Device Identification register
04h-05h	PCI Command register
06h-07h	PCI Status register
08h	PCI Revision ID register
40h	PCI Control register

HOST INTERFACE

7.5. CACHE RELATED REGISTERS

The STPC supports two caching modes, write-through and write-back. For both modes, sdram read accesses are copied into the cache, and future accesses then return the cache copy with no access to sdram. The situation is different for write access; for the write-through mode, a write updates both the sdram and the cache, whereas in the write-back mode, a write updates the cache only with the sdram update taking place later. The write-back mode offers improved performance over the write-through mode.

Two cache levels are generally available, level 1 (L1), within the CPU core, and level 2 (L2), within the chipset core (between the CPU and the sdram Controller). For the STPC product range, the L2 cache controller is included but as the required external connection pins are not provided, it is not usable. The L2 cache control registers described below are however used to configure the CPU L1 Cache architecture.

7.5.1. CACHE ARCHITECTURE REGISTER 0

This register controls various attributes of the L2 and L1 cache.

Cash_Arc0

Access =

Regoffset = 0x20h

7	6	5	4	3	2	1	0
CPU PAS	BAO	L1 WB	SRAM		L2 B	L2 WBC	L2 BC
Default value after reset = 00000000h							

Bit Number	Mnemonic	Description
Bit 7	CPU PAS	CPU pipelined access. : 0: Not supported 1: Supported
Bit 6	BAO	Burst addressing order. 0: Intel 1: Linear
Bit 5	L1 WB	L1 write back indication. 0: Not supported 1: Supported
Bit 4-3	SRAM	SRAM type. These bits control the type of SRAMs used to construct L2 cache. (See Table 7-3)
Bit 2	L2 B	Number of L2 banks. When programmed to 2 banks, L2 interleaving is enabled. 0: One bank 1: Two banks
Bit 1	L2 WBC	L2 write back control. 0: Write through 1: Write back
Bit 0	L2 BC	L2 cache enable. 0: Disabled 1: Enabled

Table 7-3. Bits 4-3 SRAM Type

Bit 4	Bit 3	L2 cache SRAM type
0	0	asynchronous SRAM
0	1	synchronous burst SRAM
1	0	synchronous burst pipelined SRAM
1	1	reserved

HOST INTERFACE

7.5.2. CACHE ARCHITECTURE REGISTER 1

This register controls various attributes of L2 cache.

Cash_Arc1

Access =

Regoffset = 0x21h

7	6	5	4	3	2	1	0
L2 CS			IO NA	S FIFO		R AWE	Rsv
Default value after reset = 00000000h							

Bit Number	Mnemonic	Description
Bits 7-5	L2 CS	L2 cache size. (See Table 7-4)
Bit 4	IO NA#Enable	IO NA# Enable. 0: Generate NA# 1: Don't generate NA#
Bits 3-2	S FIFO	Source FIFO low water mark. These bits control the degree of concurrency between a L1 cache line fill and start of the next memory access. A cache line wide read buffer is implemented. Due to pipelining, it is possible that the buffer may be filled up ahead of drain. Then if the next access is also a read from memory, these bits determine when the next read will be kicked off relative to the drain of the current line from the read buffer. The optimal value is a function of the drain rate of the buffer which depends on the cache RAM type and the programmed burst parameters. A value of '0' for this field is the least optimal value but will always work. (See Table 7-5)
Bit 1	R AWE	Read around write enable. 0: Reads can not proceed around any posted writes 1: Reads can go around a posted write if it is to a different address to the posted writes
Bit 0	Rsv	Reserved.

Table 7-4. L2 Cache Size

Bit 7	Bit 6	Bit 5	L2 Cache Size
0	0	0	64Kb
0	0	1	128Kb
0	1	0	256Kb
0	1	1	512Kb
1	0	0	1 MB
1	0	1	2 MB

Table 7-5. Source FIFO Low Water Mark

Bit 3	Bit 2	Start next read...
0	0	only after completely finishing current fill
0	1	when 1 QWORD is still to be emptied
1	0	when 2 QWORDS are still to be emptied
1	1	when 3 QWORDS are still to be emptied

HOST INTERFACE

7.5.3. CACHE ARCHITECTURE REGISTER 2

Cash_Arc2

Access =

Regoffset = 0x22h

7	6	5	4	3	2	1	0
Rsv	SHDD	CWEPW	CDHAW	BAWS		TAWS	
Default value after reset = 1111111h							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved.
Bit 6	SHDD	Slow host data driver. 0: Fast, One clock to drive the HD bus 1: Slow, two clocks to drive HD bus
Bit 5	CWEPW	Cache write enable pulse width. 0: 1 clock wide 1: 1.5 clocks wide Applicable to asynchronous SRAMs only. Must be '0' for synchronous SRAMs.
Bit 4	CDHAW	Cache data hold after write enable. 0: Data removed in the same clock as write enable trailing edge 1: Data is kept valid for 1 extra clock after write enable Must be a '1' if 1.5 clocks wide write enable pulse width is selected via bit 5 above.
Bits 3-2	BAWS	Burst access wait states. (See Table 7-6)
Bits 1-0	TAW	Tag access wait states. (See Table 7-7)

Table 7-6. Burst Access Wait States

Bit 3	Bit 2	Burst access wait states
0	0	fastest
0	1	1 clock slower than fastest
1	0	2 clocks slower than fastest
1	1	3 clocks slower than fastest

Table 7-7. Tag Access Wait States

Bit 1	Bit 0	Tag access wait states
0	0	fastest
0	1	1 clock slower than fastest
1	0	2 clocks slower than fastest
1	1	3 clocks slower than fastest

HOST INTERFACE

7.6. ADDRESS DECODE RELATED REGISTERS

The following registers are all 8-bit. They are accessed by setting the Configuration Index Port (22h) to the Configuration Index (C.I.) shown, and then reading or writing the appropriate values from the Configuration Register Data Port (23h).

7.6.1. MEMORY HOLE CONTROL REGISTER

This 8-bit register defines the enable, size, and starting address of memory hole. Any memory accesses to this memory hole are directed to PCI/ISA bus.

MEM_HOLE				Access =		Regoffset = 0x24h	
7	6	5	4	3	2	1	0
MHE	MHS			MHSA			
Default value after reset = 00000000h							

Bit Number	Mnemonic	Description
Bit 7	MHE	Memory Hole Enable. This bit controls the enable of memory hole function. 0 = disabled 1 = enabled
Bits 6-4	MHS	Memory Hole Size. These bits control the size of memory hole (See Table 7-8)
Bits 3-0	MHSA	Memory Hole Start Address. These bits control the bits 23-20 of the memory hole starting address. The memory hole starting address must be aligned to the hole size.

Table 7-8. Memory Hole Size

Bit 6	Bit 5	Bit 4	Memory Hole Size
0	0	0	1 MB
0	0	1	2 MB
0	1	1	4 MB
1	1	1	8 MB
others			reserved

Programming notes:

This memory hole is also non-cacheable.

7.6.2. SHADOW CONTROL REGISTER 0

This 8-bit register controls the read/write attributes of the memory located at C0000h-CFFFFh. Each 16k of the whole 64k is controlled by 2 bits, one for read and one for write.

SHADOW_0

Access =

Regoffset = 0x25h

7	6	5	4	3	2	1	0
RC1	WC1	RC2	WC2	RC3	WC3	RC4	WC4
Default value after reset = 00000000h							

Bit Number	Mnemonic	Description
Bit 7	RC1	Read Control CC000h-CFFFFh. This bit controls the read attribute of the CC000h-CFFFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 6	WC1	Write Control CC000h-CFFFFh. This bit controls the write attribute of the CC000h-CFFFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle
Bit 5	RC2	Read Control C8000h-CBFFFh. This bit controls the read attribute of the C8000h-CBFFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 4	WC2	Write Control C8000h-CBFFFh. This bit controls the write attribute of the C8000h-CBFFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle
Bit 3	RC3	Read Control C4000h-C7FFFh. This bit controls the read attribute of the C4000h-C7FFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 2	WC3	Write Control C4000h-C7FFFh. This bit controls the write attribute of the C4000h-C7FFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle

HOST INTERFACE

Bit Number	Mnemonic	Description
Bit 1	RC4	Read Control C0000h-C3FFFh. This bit controls the read attribute of the C0000h-C3FFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 0	WC4	Bit 0 Write Control C0000h-C3FFFFh. This bit controls the write attribute of the C0000h-C3FFFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle

Programming Notes:

There is single cacheability bit for the 32k Video BIOS segment (C0000h-C7FFFh) located in Shadow Control register 2. C7FFFFh-CFFFFh segment has the cacheability bit hardwired to '1' (enabled). If shadow is enabled for read/write cycles, read from and write to this area are directed to the system memory. Or else the cycles are forwarded to the expansion buses.

7.6.3. SHADOW CONTROL REGISTER 1

Similar to Shadow Control Register 0, this 8-bit register controls the read/write attributes of the memory located at D0000h-DFFFFh.

SHADOW_1				Access =		Regoffset = 0x26h	
7	6	5	4	3	2	1	0
SRC	SWC	SWC	SWC	SRC	SWC	SRC	SWC
Default value after reset = 00000000h							

Bit Number	Mnemonic	Description
Bit 7	SRC	Shadow Read Control DC000h-DFFFFh. This bit controls the read attribute of the DC000h-DFFFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 6	SWC	Shadow Write Control DC000h-DFFFFh. This bit controls the write attribute of the DC000h-DFFFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle
Bit 5	SWC	Shadow Write Control D8000h-DBFFFh. This bit controls the read attribute of the D8000h-DBFFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 4	SWC	Shadow Write Control D8000h-DBFFFh. This bit controls the write attribute of the D8000h-DBFFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle
Bit 3	SRC	Shadow Read Control D4000h-D7FFFh. This bit controls the read attribute of the D4000h-D7FFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 2	SWC	Shadow Write Control D4000h-D7FFFh. This bit controls the write attribute of the D4000h-D7FFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle
Bit 1	SRC	Shadow Read Control D0000h-D3FFFh. This bit controls the read attribute of the D0000h-D3FFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 0	SWC	Shadow Write Control D0000h-DFFFFh. This bit controls the write attribute of the D0000h-DFFFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle

Programming Notes: This entire 64K segment has the cacheability bit hardwired to '0' (disabled)

HOST INTERFACE

7.6.4. SHADOW CONTROL REGISTER 2

Similar to Shadow Control Register 0, this 8-bit register controls the read/write attributes of the memory located at E0000h-EFFFFh.

SHADOW_2				Access =		Regoffset = 0x27h	
7	6	5	4	3	2	1	0
RC	WC	RC	WC	RC	WC	RC	WC
Default value after reset = 00000000h							

Bit Number	Mnemonic	Description
Bit 7	RC	Read Control EC000h-EFFFFh. This bit controls the read attribute of the EC000h-EFFFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 6	WC	Write Control EC000h-EFFFFh. This bit controls the write attribute of the EC000h-EFFFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle
Bit 5	RC	Read Control E8000h-EBFFFh. This bit controls the read attribute of the E8000h-EBFFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 4	WC	Write Control E8000h-EBFFFh. This bit controls the write attribute of the E8000h-EBFFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle
Bit 3	RC	Read Control E4000h-E7FFFh. This bit controls the read attribute of the E4000h-E7FFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 2	WC	Write Control E4000h-E7FFFh. This bit controls the write attribute of the E4000h-E7FFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle
Bit 1	RC	Read Control E0000h-E3FFFh. This bit controls the read attribute of the E0000h-E3FFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 0	WC	Bit 0 Write Control E0000h-EFFFFh. This bit controls the write attribute of the E0000h-EFFFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle

Programming Notes: This entire 64K segment has the cacheability bit hardwired to '0' (disabled)

7.6.5. SHADOW CONTROL REGISTER 3

This 8-bit register controls the cacheability attributes of C0000h-C7FFFh and F0000h-FFFFFh shadow segments.

SHADOW_3			Access =			Regoffset = 0x28h	
7	6	5	4	3	2	1	0
SMRAM	CCF	CCC	Rsv			RCF	WCF
Default value after reset = 00000000h							

Bit Number	Mnemonic	Description
Bit 7	SMRAM	SDRAM Initialization Enable. This bit controls whether CPU accesses in A0000h-BFFFFh address range are decoded as VGA frame buffer access or SMRAM access. 0 = A0000h-BFFFFh is interpreted as VGA frame buffer access 1 = A0000h-BFFFFh is interpreted as SMRAM access. The STPC allows for 128KBytes of SMRAM. Physically this memory is located in the system memory behind the higher address range. This area of the system memory is normally unused since this address range is normally mapped to frame buffer which has its own memory. When the CPU is operating in SMM, accesses in the range of A0000-BFFFFh goes to SMRAM instead of VGA frame buffer. The rest of the address map remains unchanged. The address range A0000h-BFFFFh is always non-cacheable.
Bit 6	CCF	Cache Control F0000h-FFFFFh. This bit controls the cacheability of F0000h-FFFFFh block when the shadow function is enabled. 0 = cacheability disabled 1 = cacheability enabled
Bit 5	CCC	Cache Control C0000h-C7FFFh. This bit controls the cacheability of C0000h-C7FFFh block when the shadow function is enabled. 0 = cacheability disabled 1 = cacheability enabled
Bits 4-2	Rsv	Reserved.
Bit 1	RCF	Read Control F0000h-FFFFFh. This bit controls the read attribute of F0000h-FFFFFh memory. 0 = shadow disabled for read cycle 1 = shadow enabled for read cycle
Bit 0	WCF	Bit 0 Write Control F0000h-FFFFFh. This bit controls the write attribute of F0000h-FFFFFh memory. 0 = shadow disabled for write cycle 1 = shadow enabled for write cycle

Programming notes:

The rest of the shadow RAM segments have the cacheability bits hardwired to '0' (disabled). This register also provides control over the address range for which ROM chip-select (ROMCS#) will be asserted allowing various BIOSes (system, video, disk etc.) to be implemented in a single part. Bit 7 of this register also provides accessibility to the SMM mode RAM (SMRAM).

HOST INTERFACE

7.6.6. VGA DECODE REGISTER

This 8-bit register controls address decode for the internal VGA as follows:

VGA_DEC

Access =

Regoffset = 0x29h

7	6	5	4	3	2	1	0
Rsv		Rsv		DC	PSE	I VGA D	ADE
Default value after reset = 00000011h							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved.
Bit 5-4	Rsv	Reserved.
Bit 3	DC	stop d-clock (Dot clock).
Bit 2	PSE	Palette Snoop Enable: 1 = Palette write cycles are propagated to PCI bus in addition to updating the internal palette. 0 = Palette write cycles are terminated internally and are not propagated to PCI.
Bit 1	I VGA D	Internal VGA Disable. This bit if set to a '0' will disable internal VGA. Otherwise if set to a '1', it will enable the internal VGA.
Bit 0	ADE	Add-in Decode Enable. This bit if set to a '0' will map the internal VGA to add-in card address space. Otherwise if set to a '1' it will map the VGA to mother-board address space.

7.7. HOST SDRAM CONTROLLER REGISTERS

The STPC manages 4 Memory Banks (if DIMM sockets are used they can be populated with either single or double sided 64-bit data DIMMs). For SDRAM densities are supported see the datasheet [Section 6.3.3](#).

Configuration registers 30-33 provide the top addresses for each bank. Any bank can be skipped by the top addresses of two consecutive banks having the same address.

7.7.1. MEMORY BANK 0 REGISTER - C.I. 30H (MEMORY__BANK0)

This 8-bit register controls the top address of memory bank 0. Register bit 7-0 corresponding to memory address bits 27-20.

Bank 0 Top Address = Memory Bank0 size in MBytes -1.

Bank 1 Top Address = Memory Bank0 + Memory Bank1 size in MBytes -1

This register defaults to 07h.

Example 1:

Memory Bank0 = 4MB

Memory Bank1 = 4MB

Bank 0 Top Address = 4 -1= 3= 03h

Bank 1 Top Address = 4 + 4 - 1 = 07h

Bank 2, 3 Top Address = 07h

Example 2: for use with double sided DIMMs

Memory Bank0 = 32MBytes (dbl. sided DIMMS)

Memory Bank1 = 32MBytes (dbl. sided DIMMS)

Bank 0 Top Address = 16 - 1 = 15 = 0Fh

Bank 1 Top Address = 16 + 16 - 1 = 31 = 1Fh

Bank 2 Top Address = 32 + 16 - 1 = 47 = 2Fh

Bank 3 Top address = 48 + 16 - 1 = 63 = 3Fh

7.7.2. MEORY BANK 1 REGISTER - C.I. 31H (MEMORY_BANK1)

This register controls the top address of memory bank 1.

7.7.3. MEMORY BANK 2 REGISTER - C.I. 32H (MEMORY_BANK2)

This register controls the top address of memory bank 2.

7.7.4. MEMORY BANK 3 REGISTER - C.I. 33H (MEMORY_BANK3)

This register controls the top address of memory bank 3.

HOST INTERFACE

7.7.5. GRAPHICS MEMORY SIZE REGISTER

This register defines the size of SDRAM used by the graphics for frame buffer.

GRAPH_MEM

Access =

Regoffset = 0x36h

7	6	5	4	3	2	1	0
GRAS	Rsv	TGM					
Default value after reset = 00000100h							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved
Bit 6	Rsv	Reserved.
Bits 5-0	TGM	Top of Graphics Memory. This indicates frame buffer size in 128KB units. The range is 0 to 32 for 0 to 4MB framebuffer, so 6 bits are necessary.

7.7.6. SDRAM REFRESH REGISTER

This refresh register also contains a number of host clock settings for the SDRAM refresh interval.

SDRAM_Ref			Access = 0022h/0023h			Regoffset = 039h	
7	6	5	4	3	2	1	0
RE	RC						
Default value after reset = 30h							

Bit Number	Mnemonic	Description
Bit 7	RE	Refresh Enable. This bit must be programmed to '0' for normal operation
Bits 6-0	RC	Refresh Cycle. (HCLK frequency in MHz * 15.6us) >> 4

* Examples: (rounded down to nearest integer)

$\text{round_down}(75\text{MHz} * 15.6\mu\text{s}) \gg 4 = 73 = 49\text{h}$

$\text{round_down}(66\text{MHz} * 15.6\mu\text{s}) \gg 4 = 65 = 41\text{h}$

$\text{round_down}(60\text{MHz} * 15.6\mu\text{s}) \gg 4 = 58 = 3\text{Ah}$

$\text{round_down}(50\text{MHz} * 15.6\mu\text{s}) \gg 4 = 48 = 30\text{h}$

Programming notes:

The refresh interval should be reset to the smallest likely run time value (typically 48 HCLKs) to provide warm up cycles for the SDRAM.

A refresh request is generated whenever this register is written to without setting the refresh enable bit.

HOST INTERFACE

7.7.7. PRESENTS DETECT REGISTER - C.I. 97H

This register is read through the DDC register in [Section 12.9.30.](#) .

7.8. ACCESSING CONFIGURATION REGISTERS

The Host interface and the Local Bus Interface are programmed identically. To access all the internal configuration registers, the programmer will need to program the Index (address) and data registers of the the required interface through port 22h/23h. The principle of the programming is to fix the address of device to a location that the user requires and to always adress it at that location. The steps required to access any of the internal registers are as follows:

1. Select the interface you want to programme. Each interface is described as a device and both have a number. The Local Bus device number is 6 and the Host device number is 7. The below example code describes how the devices are accessed and the Host device is used.

2. Select Host interface base programming option in RBI, by writing 0x00 and 0x07 (0x06 for the Local Bus, see [Section 11.4.](#) for more details) in register 0x11 (index value 0x11 accessed through I/O 22h/23h address) and 0x10 respectively.

```
IOWRITE8(0x22,0x10);
```

```
IOWRITE8(0x23,0x07);
```

```
IOWRITE8(0x22,0x11);
```

```
IOWRITE8(0x23,0x00);
```

3. Select the Host interface address. Assume that HOST_BASE is the address of the Host interface I/O space.

```
IOWRITE8(0x22,0x12);
```

```
IOWRITE8(0x23,(HOST_BASE &0xFF) | 0x03);
```

```
IOWRITE8(0x22,0x13);
```

```
IOWRITE8(0x23,HOST_BASE >>8);
```

The host interface registers are then accessed with HOST_BASE as the index register and HOST_BASE+4 as the data register, as shown below.

4. Writing into any Internal Register of the Host Interface:

```
IOWRITE8(HOST_BASE,offset);
```

```
IOWRITE32(HOST_BASE+4,data);
```

Here the “offset” index address is as mentioned in the register table shown above. The 32-bit “data” is written into the register.

5. Reading from any internal register of Host Input

```
IOWRITE8(HOST_BASE,offset);
```

```
IOREAD32(HOST_BASE+4,data);
```

Here the “offset” index address is as mentioned in the register tables shown above. The 32-bit “data” is expected to be read from the internal register.

One constraint is that the Local Bus address must be set at multiples of 8h.

8. SDRAM CONTROLLER

8.1. INTRODUCTION

This chapter describes the mapping of the CPU memory and IO address spaces.

The STPC uses a Unified Memory Architecture; the system memory and the graphics buffers use the same memory space. This chapter provides information on the memory address map and the graphics memory usage, together with information on the arbitration logic which resolves accesses to the main memory. Details of memory shadowing and cachability by software control and the Memory Hole for ISA BIOS are also given. The actual interface to the external SDRAM modules is presented. Also introduced in this chapter are the PCI configuration space mapping registers, further details are in the chapter relating to the PCI Bus Controller.

8.2. MEMORY CONTROLLER

The STPC handles the memory data bus directly, controlling from 8 MBytes to 128 MBytes. The SDRAM controller supports accesses to the Memory Banks to/from the CPU (via the host), from the VIP, to/from the CRTC, and to the VIDEO with Video Pipeline & to/from the GE (Banks 0 to 3), and the local Bus which can be populated with either single-sided or double-sided 72-bit (4-bit parity) memory devices. Parity is not supported.

The SDRAM controller only supports 64 bit wide Memory Banks.

The SDRAM Controller supports buffered or unbuffered SDRAM but not EDO or FPM modes. SDRAMs must support Full Page Mode Type access.

The STPC Memory Controller provides various programmable SDRAM parameters to allow the SDRAM interface to be optimised for different processor bus speeds SDRAM speed grades and CAS Latency.

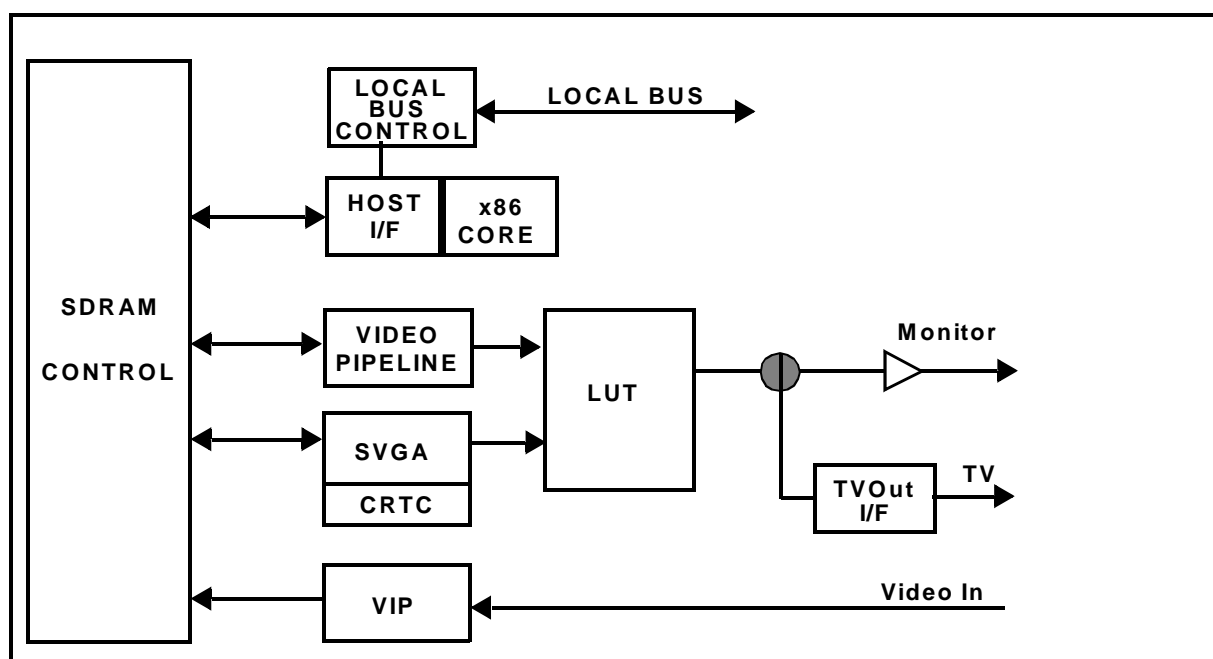


Figure 8-1. Memory Controller Interface Block Diagram

SDRAM Controller

8.3. SDRAM REGISTER ACCESS

These registers are used to configure the SDRAM controller.

8.3.1. REGISTER 0

This is a 31-bit configuration register for the SDRAM controller block:

MEM_REG0				Access =								Regoffset = 84C6000h			
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RCASLCY			REGD	MRS R	RASo	LHDI	LGDI	LCDI	CASLat			Config		PRA
Default value after reset = 31x32198376h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRA	Rsv				RRW			BT	BL			RCT			
Default value after reset = 31x32198376h															

Bit Number	Mnemonic	Description
Bits 30-28	RCASLCY	Read CAS Latency (RCASLCY) should be equal to CASLCY but is left programmable for debug purpose.
Bit 27	REGD	Registered DIMM , Indicate if we use registered DIMMs '1' or not '0'.
Bit 26	MRSR	Mode Register Set Request , If set to 1, we update the SDRAM chips corresponds to the value programmed Bits [16:0].
Bit 25	RASo	RAS on/off , When we finish a read or a write, if set to 1 go into RACTIVE, if set to 0, go into PRECHARGE and the IDLE.
Bit 24	LHDI	Latch_Host_Data_In for host input data. If set to 0, select MD[63:0] directly from SDRAM, if set to 1, select latched MD[63:0] by RDCLK (see bits 3-0 in Register 1).
Bit 23	LGDI	Latch_GE_Data_In for GE input data. If set to 0 it selects MD[63:0] directly from SDRAM, if set to 1 it selects latched MD[63:0] by RDCLK (see bits 3-0 in Register 1)
Bit 22	LCDI	Latch_CRTC_Data_In for CRTC input data. If set to 0, it select MD[63:0] directly from SDRAM, if set to 1 it selects latched MD[63:0] by RDCLK (see bits 3-0 in Register 1).
Bits 21-19	CASLat	CAS Latency This is abbreviated as CL in SDRAM datasheets and is defined as the number of clock cycles for the data held for after CAS goes low.

Bit Number	Mnemonic	Description
Bits 18-17	Config	CONFIGURATION of a DIMM. (See Table 8-1) These bits are used to determine the maximum burst length (full page burst). If the DIMMS are populated with a different kind of memory, the 2 bits are programmed to maximise the burst length using the minimum amount of the memory.
Bits 16-15	PRA	Precharge to Row Active number of cycles (called tRP in datasheets).
Bits 14-11	Rsv	Reserved. Should be set to '0000'.
Bits 10-8	RRW	RACTIVE to Read/Write (Called tRCD in datasheets).
Bit 7	BT	Burst Type. Should be set to '0'.
Bits 6-4	BL	Burst Length. Should be set to '111'
Bits 3-0	RCT	Refresh Cycle Timing (Called tRC in SDRAM datasheets).

Table 8-1. Memory Bank Configuration

Bit 18	Bit 17	Memory Bank Configuration	Maximum Burst Length
0	0	[4Mx4]x16	1024
0	1	[2Mx8]x8	512
1	0	[1Mx16]x4	256
1	1	Reserved	

SDRAM Controller

8.3.2. REGISTER 1

This 6-bit register is used for the read clock scheme. See Chapter 6.3 "Clock considerations" for more details. This delay can be set up to 3.5 ns beyond the 15ns required from the previous MCLKI edge.

MEM_REG1

Access =

Regoffset = 84C6004h

	5	4	3	2	1	0
	CSMEM	MEM	RCDP			
Default value after reset = 000000h						

Bit Number	Mnemonic	Description
Bit 5	CSMEM	CS_MEM16_OE It is programmed as bit 4 in case of 64Mbits and 128Mbits and is programmed to 1 otherwise.
Bit 4	MEM	MEM16_OE_ , This bit is set to '1' to get 16mA output enabled, set to '0' to get 8mA output enabled
Bits 3-0	RCDP	Read Clock Delay Programming , 0000 for smallest delay to 1111 for largest delay

8.3.3. REGISTER 2 (MEM_REG2) 84C6008H

This 2-bit register is used to determine the type of SDRAM in use.

MEM_REG2	Access =	Regoffset = 84C6008h	
Empty		1	0
Empty		SDRAM	
Default value after reset = 000000h			

Bit Number	Mnemonic	Description
Bits 1-0	SDRAM	SDRAM type. (See Table 8-2)

Table 8-2. SDRAM Type

Bit 1	Bit 0	Description
0	0	16 Mbits SDRAMs
0	1	64 Mbits or 128 Mbits 2 SDRAM banks
1	0	64 Mbits or 128 Mbits 4 SDRAM banks

SDRAM Controller

8.4. MEMORY CLOCK REGISTERS

The MCLK register is used for Memory Clock control operations.

8.4.1. MCLK CONTROL REGISTER 0

MCLK00

Access =

Regoffset = 0x40h

7	6	5	4	3	2	1	0
Uns	4-bitDIV				8-bitP		
Default value after reset = 0x5B							

Bit Number	Mnemonic	Description
Bit 7	Uns	Unused.
Bits 6- 3	4-bitDIV	This is the 4-bit M (divisor) value of the Memory synthesiser.
Bits 2-0	8-bitN	This is the 3-bit P (exponent) value of the Memory clock synthesizer.

This register defaults to 0x5B at reset. This value when combined with the default value of the other half of this pair results in a memory clock of 80.05 MHz assuming 14.318 MHz oscillator clock as the reference input.

For MCLK frequency programming values see table below:Table 8-3.

Note: If programming MCLK to a frequency not equal to HCLK, strap MD[5] must be disabled (i.e. set to 0) to remove the synchronization between these two clock signals (see Atlas Datasheet, STRAP OPTION section for further details).

$$MCLK = \frac{2 \times 14.31818 \times N}{M \times 2^P}$$

Constraints: $1 \leq M \leq 255$
 $1 \leq N \leq 255$
 $0 \leq P \leq 5$

$$1 \text{ MHz} \leq \frac{14.31818}{M} \leq 2 \text{ MHz}$$

$$200 \text{ MHz} \leq \frac{2 \times 14.31818 \times N}{M} \leq 622 \text{ MHz}$$

8.4.2. MCLK CONTROL REGISTER 1

MCLK01

Access =

Regoffset = 0x41h

7	6	5	4	3	2	1	0
8-bitN							
Default value after reset = 0xEC							

Bit Number	Mnemonic	Description
Bits 7- 0	8-bitN	These are bits 4-0 of the 8-bit N (multiplier) value of the Memory clock synthesiser.

This register defaults to 0xEC at reset. This value when combined with the default value of the other half of this pair results in a memory clock of 80.05 MHz assuming 14.318 MHz oscillator clock as the reference input.

For MCLK frequency programming values see [Table 8-3](#)

Table 8-3. MCLK Control Register Address 22 Index 40h, 41h

MHz	Reg1, Index 41h	Reg0, Index 40h	Actual Freq.	m	n	p
100	9Ah	5Ah	100.227260	11	9Ah	2
95	92	5Ah	95.020649	11	146	2
90	B0h	72h	89.999989	14	176	2
85	5Fh	42h	85.014194	8	95	2
80	7Bh	5Ah	80.051643	11	123	2
75	88h	6Ah	74.895095	13	136	2
66	95h	43h	65.965901	8	149	3
60	6Dh	6Ah	60.026216	13	109	2
55	A9h	5Bh	54.994828	11	169	3
50	4Dh	5Ah	50.113630	11	77	2
45	B0h	73h	44.999994	14	176	3
8	3Fh	3Dh	8.053978	7	63	5

8.5. SDRAM ARBITRATION:

Several agents, i.e. CPU, PCI masters, ISA masters, Graphics engine, CRT controller, Video Output, Video Input Port and Refresh controller, all compete for the system SDRAM memory.

A hierarchical arbitration scheme is used to optimise the SDRAM bandwidth usage. The system arbiter arbitrates among CPU, PCI and ISA masters. Refer to system arbiter section of this specification for details of how this is done. The winner of this arbitration, the system master, competes with the remaining agents for SDRAM. The SDRAM arbiter employs a dynamic arbitration algorithm to optimise the SDRAM utilization. The arbiter behaviour changes depending on whether the scan is close to and during the display of the video window:

- The following rules apply when the scan is not close to the video window.
- Refresh request is the lowest priority and is serviced only if no other agent is actively requesting.
- CRTC requests while current occupancy of the FIFO is above the low water mark are the next lowest priority requests and can be arbitrated out by GE, CRTC or video requests.
- CRTC requests when the occupancy is below the low water mark (urgent requests) have the highest priority will win over all other agents.
- Graphics engine requests lose to urgent CRTC and System master request. A System master request will terminate an ongoing Graphics service at the nearest CAS boundary while a CRTC request can terminate a on-going graphics service at the end of a sequence of read/write.
- The Video Output requests not close to the video window are prioritised just above the refresh.

When the scan is close to the video window and during the video window display, the arbiter behaviour changes significantly. The goal of the arbiter here is to ensure that the CRTC and Video FIFO occupancy is above a programmable minimum number of Bytes. This is necessary because, some memory and screen configurations do not have sufficient bandwidth availability. Since the drain rate is equal to the peak available bandwidth, it can not be sustained if all the pixels are to be fetched on demand. To overcome this, the arbiter ensures that a reservoir of CRTC and video pixels is available before the video window scan starts so that the difference of the fetch and drain rates can be made up for by dipping into this reservoir. This reservoir thus progressively shrinks as the video window is painted and approaches 0 Bytes by the end of the video window.

To ensure that the reservoir is filled up, a programmable distance before the video window x position, the arbiter switches over to a different set of low water marks for determining the urgency of the CRTC and video requests. Once urgent, these requests win over other requesters thus ensuring that the reservoir is full. Further, to avoid thrashing between CRTC and Video requests, the arbiter employs a programmable burst length to arbitrate between the two. Once the CRTC service is started, it is not interrupted by video until the burst length number of cycles have occurred and vice-versa. Since the drain rates of video changes with the scaling factor, the CRTC and video have different burst length parameter.

Once the video window repaints starts, the low water marks decrease linearly over the size of the window, to reflect the decreasing number of reservoir Bytes needed to make up for the difference in the fetch and drain rates. All other memory requesters are granted access, only if both CRTC and video FIFO occupancies are above their low water marks. The rules for granting the memory to the remaining agents are same as those listed above.

9. PCI CONTROLLERS

9.1. INTRODUCTION

The PCI bus is the main data communication link to the STPC chip. Two PCI devices are present internally in the STPC, a “North Bridge” and a “South Bridge”. The STPC also contains a PCI arbiter which arbitrates between the two bridges and for up to three external PCI devices. [Figure 9-1](#) below shows the layout of the PCI controllers within the STPC. Please refer to *PCI Specification 2.1*, from PCI-SIG, for further details of the PCI bus standard.

The *North Bridge* translates the appropriate host bus I/O and Memory cycles to the PCI bus. It also supports generation of Configuration cycles on the PCI bus. The Configuration Address register allows for the remapping of host CPU I/O cycles, in the address range 0xCF8h-0xCFFh, to configuration cycles on the PCI bus.

The North Bridge, as a PCI bus agent (host bridge class), fully complies with PCI specification 2.1. The North Bridge also implements the PCI mandatory header registers in Type 0 PCI configuration space for easy porting of PCI-aware system BIOS. The North Bridge is assigned the Device Number 0xBh, which corresponds to the IDSEL on AD11 signal. PCI configuration registers of the North Bridge are accessible by the Type 0 PCI configuration cycles generated at Device number 0xBh.

The *South Bridge* controller responds to PCI configuration read and write transactions. The South Bridge is assigned the Device Number 0Ch, which corresponds to the IDSEL on AD12 signal. PCI configuration registers of the South Bridge are accessible by the Type 0 PCI configuration cycles generated by the North Bridge.

The South Bridge, as a PCI bus agent (expansion bridge class), fully complies with PCI specification 2.1. The South bridge implements two PCI functions:

- Function 0, PCI to ISA bridge,
- Function 1, IDE controller.

As per the PCI specification, the South Bridge will respond to both function 0 and function 1 configuration cycles directed to configuration slot 12 (AD12).

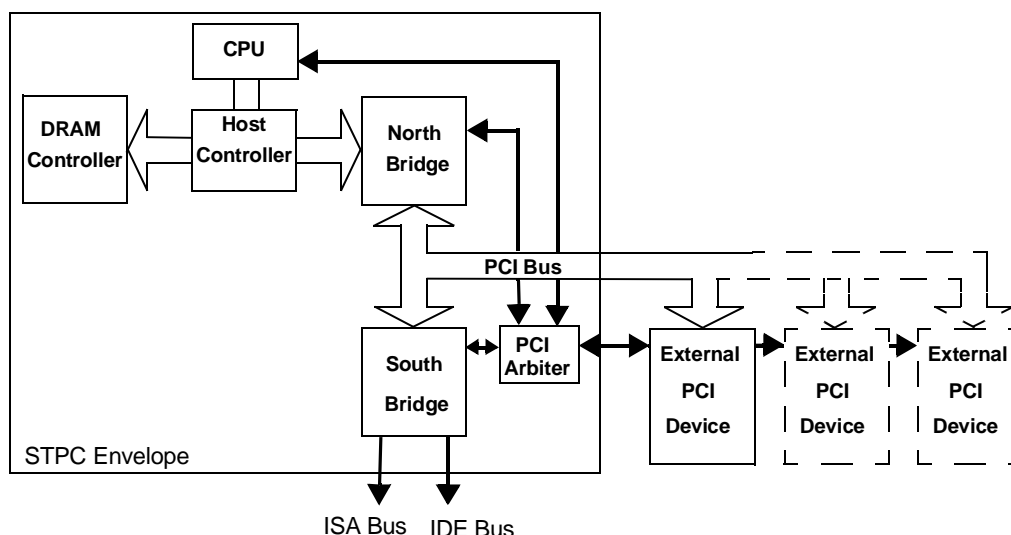


Figure 9-1. PCI Layout

PCI CONTROLLERS

9.1.1. PCI ADDRESS DECODE

The only positive decode carried out is for the IDE controller PIO registers. The decode address ranges are dictated by the IDE configuration registers, see IDE section for details. ISA resources are accessed only via subtractive decode.

9.1.2. PCI ERROR HANDLING

Under control of South Bridge configuration registers, one or more of the following events can generate a 1 PCICLK long pulse on SERR#, which in turn can be made to generate an NMI to the CPU.

ISA initiated transaction ending in target abort.

9.1.3. PCI ARBITER

The PCI arbiter controls access to the PCI bus when several bus masters are present in the system. Whenever a further potential bus master needs to gain access to the bus, it asserts its request. The arbiter then asserts a system hold condition, which eventually causes a hold signal to be asserted to the CPU. The CPU finishes the current instruction, tristates the internal bus and asserts a hold acknowledge. This eventually causes the assertion of a system hold acknowledge. Once the system hold acknowledge is asserted, the arbiter asserts a grant to whichever requesting master is in the front of the line in a round-robin chain. When there are no requests pending or when the CPU is requesting the bus and it is in the front of the line, control of the bus is passed back to the CPU by the negation of the system hold condition.

9.2. ACCESSING THE PCI CONFIGURATION REGISTERS

The PCI configuration registers are accessed, from the CPU, using two 32-bit registers, mapped as I/O at CF8h and CFCh.

Each read from and write to the PCI configuration registers must be done by:

Writing the 32-bit address of the PCI config. register using type 0 format at I/O CF8h.

Reading or Writing 32-bit data at CFCh

All PCI configuration registers, inside the North and South bridges and all other external PCI devices, are seen from the CPU through those 2 x 32-bit registers.

An illustration of these registers is shown in [Table 9-1](#) & [Table 9-2](#).

Table 9-1. Register CF8h

31	30 ----- 24	23 ----- 16	15 ----- 11	10 ----- 8	7 ----- 2	1 0
Enable	Reserved	Bus number	Device number	Function number	Register number	0

Table 9-2. Register CFCh

31 ----- 24	23 ----- 16	15 ----- 8	7 ----- 0
Byte 3	Byte 2	Byte 1	Byte 0

9.3. CONFIGURATION ADDRESS REGISTER

This is a 32-bit register accessible only via double-word IO read and write cycles.

Config_Address

Access = 0xCF8h

Regoffset =

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI	Rsv							BN							
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DN					FN			RG						Rsv	
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bit 31	PCI	PCI configuration register access enable. When set to a '1', host CPU I/O cycles in address range CFCh-CFFh are converted to configuration cycles on the PCI bus. Otherwise if set to a '0', I/O cycles in this address range pass through as normal I/O cycles on the PCI bus.
Bits 30-24	Rsv	Reserved. Must be written to '0'. Read back as '0'.
Bits 23-16	BN	Bus Number. This field selects a specific bus number in the system. Bus Number 0 is assigned to the PCI bus directly behind the North Bridge. This field is driven on bits 23-16 of the AD bus during the address phase.
Bits 15-11	DN	Device Number. This field selects a specific device on the bus. During a Type-0 configuration cycle, this field is decoded to assert the appropriate IDSEL line as follows; The North Bridge Device Number 0xBh, which corresponds to IDSEL on AD11. The South Bridge Device Number 0xCh, which corresponds to IDSEL on AD12.
Bits 10-8	FN	Function Number. During a PCI configuration cycle, this field is driven on bits 10-8 of the AD bus of the PCI during the address phase. Function 0: PCI to ISA bridge, Function 1, IDE controller.
Bits 7-2	RG	Register Number. During a PCI configuration cycle, this field is driven on bits 7-2 of the AD bus during the address phase.
Bits 1-0	Rsv	Reserved. Must be written to a '0'. Reads back as '0'.

9.5.1. NORTH BRIDGE PCI COMMAND REGISTER

This is the 16-bit PCI command register.

NB_Com

Access = 0xCF8h/0xCFCh

Regoffset = 0x4h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv							S	AD	P	VGA	MW	ES	BS	ME	IO E
Default value after reset = 0007h															

Bit Number	Mnemonic	Description
Bits 15-9	Rsv	Reserved. These bits are hardwired to '0'. Writes have no effect on them.
Bit 8	S	SERR# enable. If this bit is set to a '1', the North Bridge may assert SERR# upon detecting a target abort in response to an North Bridge initiated PCI transaction, upon being forced to end a non-configuration space transaction with a master abort, or if a parity error on the PCI bus is detected. If this bit is set to '0', the North Bridge will not assert SERR#.
Bit 7	AD	Address/Data stepping enable. This bit is hardwired to a '0'. Writes to it have no effect.
Bit 6	P	PERR# response. Must always be set to '0'.
Bit 5	VGA	VGA Palette Snoop enable. This bit is hardwired to a '0'. Writes to it have no effect.
Bit 4	MW	Master Write and Invalidate Enable. This bit is hardwired to a '0'. Writes to it have no effect.
Bit 3	ES	Enable Special cycles. This bit is hardwired to a '0'. Writes to it have no effect.
Bit 2	BS	Bus Master enabled. This bit is hardwired to a '1'. Writes to it have no effect.
Bit 1	ME	Memory Enable. This bit is hardwired to a '1'. Writes to it have no effect.
Bit 0	I/O E	I/O Enable. This bit is hardwired to a '1'. Writes to it have no effect.

PCI CONTROLLERS

9.5.2. NORTH BRIDGE PCI STATUS REGISTER

This is the 16-bit PCI Status register.

NB_Stat

Access = 0xCF8h/0xCFCh

Regoffset = 0x6h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DP	SS	SMA	RTA	STA	DT		DPED	FBBC	Rsv						
Default value after reset = 0280h															

Bit Number	Mnemonic	Description
Bit 15	DP	Detected parity error. This bit is set when a PCI parity error is detected. It may be cleared by software by writing a '1' back to this bit.
Bit 14	SS	Signalled SERR#. This bit is set to a '1' when SERR# is asserted by the North Bridge. Writing a '1' to this bit will clear it.
Bit 13	SMA	Signalled Master Abort. This bit is set to a 1 when the North Bridge terminates a PCI transaction with a master abort. Writing a '1' to this bit will clear it.
Bit 12	RTA	Received Target Abort. This bit is set to a '1' when PCI transaction initiated by the North Bridge is terminated with a target abort. Writing a '1' to this bit will clear it.
Bit 11	STA	Signalled Target Abort. This bit is hardwired to '0'.
Bits 10-9	DT	DEVSEL Timing. These bits are hardwired for medium timing to '01'. Writes have no effect.
Bit 8	DPED	Data Parity Error Detected. This bit is set to '1' when a PCI data parity error is detected. Writing a '1' will clear it.
Bit 7	FBBC	Fast Back-to-Back Capable. Hardwired to '1'. Indicates that the North Bridge, while acting as target, is capable of accepting fast back-to-back transactions. Reads will always return '1', writes have no effect.
Bits 6-0	Rsv	Reserved. These bits are hardwired to '0's.

9.5.3. NORTH BRIDGE PCI REVISION ID REGISTER

This is the 8-bit read only PCI revision identification register.

<i>NB_R_ID</i>		Access = 0xCF8h/0xCFCh				Regoffset = 0x8h	
7	6	5	4	3	2	1	0
Rsv							
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-0	Rsv	Reserved. These bits are hardwired to 00h.

PCI CONTROLLERS

9.5.4. NORTH BRIDGE DEVICE CLASS CODE REGISTER

This is a 24-bit read only register implemented at configuration space offset 9h, Ah, Bh.

NB_C_Code

Access = 0xCF8h/0xCFCh

Regoffset = 0x9h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCC								SCC							
Default value after reset = 00h								Default value after reset = 00h							

15	14	13	12	11	10	9	8
PIR							
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 31-24	BCC	Base Class Code. These bits are hardwired to 00h.
Bits 23-16	SCC	Sub Class Code. These bits are hardwired to 00h.
Bits 15-8	PIR	Programming Interface Register. These bits are hardwired to 00h.

9.5.5. NORTH BRIDGE HEADER TYPE REGISTER

This is an 8-bit read only register, hardwired to 00h

NB_Head

Access = 0xCF8h/0xCFCh

Regoffset = 0xEh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

PCI CONTROLLERS

9.5.6. NORTH BRIDGE CONTROL REGISTER

NB_Cont

Access = 0xCF8h/0xCFCh

Regoffset = 0x50h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv									PCI1	PCI2	PCI3	Rsv			
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv											P			SP	S
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-23	Rsv	Reserved. Hardwired to '0'.
Bit 22	PCI1	PCI 2.0 Enable. If this bit is set to '1', North Bridge will be compatible with PCI 2.0 standard. If this bit is set to '0', North Bridge is compatible with PCI 2.1 standard.
Bit 21	PCI2	PCI to Host Read Prefetch Enable. If this bit is set to '1', all QWORD aligned burst reads from a PCI master addressed to the North Bridge system memory will use prefetch. If set to '0', memory read cycles from PCI to host are allowed to complete before the PCI cycle is terminated and all burst read attempts will be disconnected on the PCI bus.
Bit 20	PCI3	PCI to Host Write Posting Enable. If this bit is set to '1', all burst writes from a PCI master addressed to the North Bridge system memory will be posted. If it is set to '0', all memory write cycles from PCI to host are allowed to complete before the PCI cycle is terminated and all burst write attempts will be disconnected on the PCI bus.
Bits 19-5	Rsv	Reserved. Hardwired to '0'.
Bit 4	P	PERR_ on read data parity error enable.
Bit 3	P	PERR_ on write data parity error enable.
Bit 2	P	PERR_ on address parity error enable.
Bit 1	SP	SERR_ on PERR_ enable.
Bit 0	S	SERR_ on received target abort.

9.5.7. NORTH BRIDGE PCI ERROR STATUS REGISTER

NB_E_Stat

Access = 0xCF8h/0xCFCh

Regoffset = 0x54h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv															
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv											RDP	WDP	AP	PES	RTAE
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-5	Rsv	Reserved. Hardwired to '0'.
Bit 4	RDP	Read Data Parity Error Status. This bit is set when a PCI read data parity error is detected. Writing a '1' will clear it.
Bit 3	WDP	Write Data Parity Error Status. This bit is set when a PCI write data parity error is detected. Writing a '1' will clear it.
Bit 2	AP	Address Parity Error Status. This bit is set when a PCI address parity error is detected. Writing a '1' will clear it.
Bit 1	PES	Parity Error Status. System errors as a result of a parity error status. This bit is set to '1' when SERR# was asserted as a result of parity error. Writing a '1' will clear it.
Bit 0	RTAE	Received Target Abort Error. System errors as a result of a received target abort. This bit is set to '1' when SERR# was asserted as a result of receiving a target abort. Writing a '1' will clear it.

PCI CONTROLLERS

9.6. THE SOUTH BRIDGE

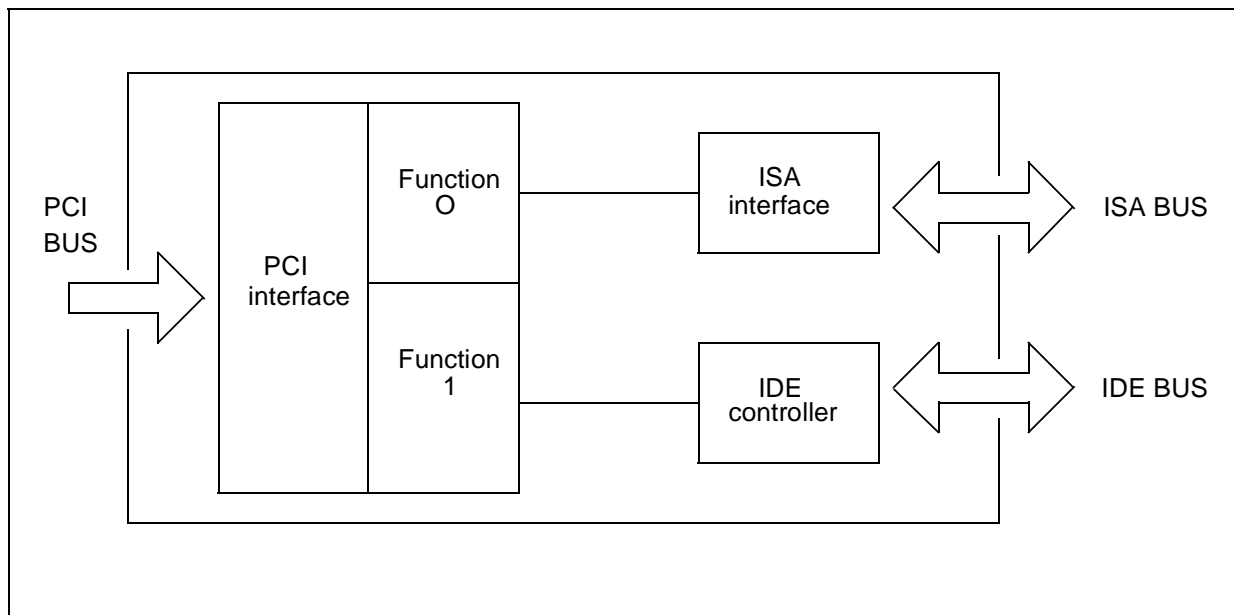


Figure 9-2. South Bridge Layout

Figure 9-2 Illustrates the South Bridge layout and the associated functions.

The STPC South Bridge configuration registers are accessed using the values below :

Bus = 0

Device = Ch (IDSEL internally connected to PCI address line 12)

Function = 0 (ISA bridge)

- Responds to I/O / memory / config
- Translates Master ISA to PCI
- Translates PCI to Slave ISA

Function = 1 (IDE controller)

- Responds to IO / config

For example: Writing 80006110h at CF8h will access Function 1 (IDE) Command reg. index.

9.7. SOUTH BRIDGE PCI FUNCTION 0 (PCI to ISA) CONFIGURATION REGISTERS

Table 9-4. Function 0 (ISA Bridge) Configuration Space Register Reset Values

31		16 15		0	
Device ID: 020Bh		Vendor ID: 104Ah		00h	
Status: 0280h		Command: 000Fh		04h	
Base class code: 06h	Sub class code: 01h	Program. Inter. Reg. : 00h	Revision ID: 00h	08h	
	Header: 80h			0Ch	
				...	
				...	
				...	
			Miscellaneous reg : 00h	40h	

This section describes Function 0 (F#0) configuration registers, including the PCI to ISA bridge control. The registers and reset values are illustrated in [Table 9-4](#).

PCI CONTROLLERS

9.7.1. SOUTH BRIDGE PCI COMMAND REGISTER

This is the 16-bit PCI command register.

SB_Com_0

Access = 0xCF8h/0xCFCh

Regoffset = 0x4h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv							S	AD	P	VGA	MW	ESC	BM	ME	I/O E
Default value after reset = 000Fh															

Bit Number	Mnemonic	Description
Bits 15-9	Rsv	Reserved. These bits are hardwired to '0's. Writes have no effect on them.
Bit 8	S	SERR# enable. If this bit is set to a '1', the South Bridge may assert SERR# upon detecting a target abort in response to a South Bridge initiated PCI transaction on behalf of an ISA master. If this bit is set to '0', the South Bridge will not assert SERR#.
Bit 7	AD	Address/Data stepping enable. This bit is hardwired to a '0'. Writes to it have no effect.
Bit 6	P	PERR# response. Setting this bit to '1' enables parity error detection.
Bit 5	VGA	VGA Palette Snoop enable. This bit is hardwired to a '0'. Writes to it have no effect.
Bit 4	MW	Master Write and Invalidate Enable. This bit is hardwired to a '0'. Writes to it have no effect.
Bit 3	ESC	Enable Special Cycles. This bit is hardwired to a '1'. The South Bridge writes to it have no effect. The South Bridge responds to halt and shutdown cycles.
Bit 2	BM	Bus Master enabled. This bit is hardwired to a '1'. Writes to it have no effect.
Bit 1	ME	Mem Enable. This bit is hardwired to a '1'. Writes to it have no effect.
Bit 0	I/O E	I/O Enable. This bit is hardwired to a '1'. Writes to it have no effect.

9.7.2. SOUTH BRIDGE PCI STATUS REGISTER

This is the 16-bit PCI Status register.

SB_Stat0

Access = 0xCF8h/0xCFCh

Regoffset = 0x6h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv	SS	SMA	RTA	STA	DT		DPED	FBBC	Rsv						
Default value after reset = 0280h															

Bit Number	Mnemonic	Description
Bit 15	Rsv	Reserved. This bit is hardwired to '0'.
Bit 14	SS	Signalled SERR#. This bit is set to a '1' when SERR# is asserted by the South Bridge on behalf of an ISA master cycle. Writing a '1' to this bit will clear it. SERR# is asserted in response to a target abort during an ISA master cycle on PCI bus and if bit-8 of the F#0 PCI command register is set to a '1' to enable SERR# signalling.
Bit 13	SMA	Signalled Master Abort. This bit is hardwired to a '0'.
Bit 12	RTA	Received Target Abort. This bit is set to a '1' when the PCI transaction is initiated by the South Bridge on behalf of an ISA master is terminated with a target abort. Writing a '1' to this bit will clear it.
Bit 11	STA	Signalled Target Abort. This bit is set to a '1' when the South Bridge terminates a PCI transaction with a target abort. Writing a '1' to this bit will clear it. The South Bridge will generate target abort if a A1-0 of a PCI IO cycle does not match the Byte enables.
Bits 10-9	DT	DEVSEL Timing. These bits are hardwired for medium timing to '01'. Writes have no effect.
Bit 8	DPED	Data Parity Error Detected. This bit is hardwired to '0'.
Bit 7	FBBC	Fast Back-to-Back Capable. Hardwired to '1'. Indicates that the South Bridge, while acting as target, is capable of accepting fast back-to-back transactions. Reads will always return '1', writes have no effect.
Bits 6-0	Rsv	Reserved. These bits are hardwired to '0'.

PCI CONTROLLERS

9.7.3. SOUTH BRIDGE PCI REVISION ID REGISTER

This is the 8-bit read only PCI revision identification register.

<i>SB_R_ID0</i>		Access = 0xCF8h/0xCFCh				Regoffset = 0x8h	
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bits 7-0: These bits are hardwired to 00h.

9.7.4. SOUTH BRIDGE DEVICE CLASS CODE REGISTER

This is a 24-bit read only register implemented at configuration space offset 09h, 0Ah, 0Bh.

SB_C_Code0

Access = 0xCF8h/0xCFCh

Regoffset = 0x9h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCC								SCC							
Default value after reset = 06h								Default value after reset = 01h							

15	14	13	12	11	10	9	8
PIR							
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 31-24	BCC	Base Class Code. These bits are hardwired to 06h (Bridge Device).
Bits 23-16	SCC	Sub Class Code. These bits are hardwired to 01h (ISA Bridge).
Bits 15-8	PIR	Programming Interface Register. These bits are hardwired to 00h.

PCI CONTROLLERS

9.7.5. SOUTH BRIDGE HEADER TYPE REGISTER

This register is hardwired to 80h, indicating that the South Bridge is a multi-function PCI device.

SB_Head0

Access = 0xCF8h/0xCFCh

Regoffset = 0xEh

7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0



9.7.6. SOUTH BRIDGE MISCELLANEOUS REGISTER

SB_Misc0

Access = 0xCF8h/0xCFCh

Regoffset = 040h

7	6	5	4	3	2	1	0
Rsv							PCI
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7-1	Rsv	Reserved. Hardwired to 00h.
Bit 0	PCI	PCI 2.0 Enable. If this bit is set to '1', South Bridge will be compatible with PCI 2.0 standard. If this bit is set to '0', South Bridge is compatible with PCI 2.1 standard.

PCI CONTROLLERS

9.8. SOUTH BRIDGE PCI FUNCTION 1 CONFIGURATION REGISTERS

This section describes the Function 1 (F#1) configuration registers. The registers and reset values are illustrated in [Table 7-16](#).

Table 9-5. Function 1 (IDE Bridge) PCI Configuration Space Register Reset Values

31	16 15		0	
Device:		Vendor ID: 104Ah		00h
Status: 0280h		Command: 0000h		04h
Base class code: 01h	Sub class code: 01h	Program. Inter. Reg. : 8Ah	Revision ID: 00h	08h
	Header: 80h	Reserved: 00h		0Ch
IO Base address 0 register: 00000001h				10h
IO Base address 1 register: 00000001h				14h
IO Base address 2 register: 00000001h				18h
IO Base address 3 register: 00000001h				1Ch
Reserved				20h
				...
				...
Primary IDE Timing register: 97609760h				40h
Secondary IDE Timing register: 97609760h				44h
			Miscellaneous reg : 00h	48h

9.8.1. SOUTH BRIDGE VENDOR IDENTIFICATION REGISTER

This is a 16-bit read-only register implemented at configuration space offset 00h and 01h. It contains the Vendor Identifier assigned to STPC.

Bits 15-0: These bits are hardwired to 100Eh.

SB_V_ID1

Access = 0xCF8h/0xCFCh

Regoffset = 0x0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0

Writes to this register have no effect.

PCI CONTROLLERS

9.8.2. SOUTH BRIDGE DEVICE IDENTIFICATION REGISTER

This is a 16-bit read only register implemented at configuration space offset 02h and 03h. It contains the Device Identifier assigned to the South Bridge.

Bits 15-0: These bits are hardwired to 55CCh

<i>SB_D_ID1</i>																Access = 0xCF8h/0xCFCh						Regoffset = 0x2h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0										
0	1	0	1	0	1	0	1	1	1	0	0	1	1	0	0										

Writes to this register have no effect.

9.8.3. SOUTH BRIDGE PCI COMMAND REGISTER

This is the 16-bit PCI command register.

SB_Com1

Access = 0xCF8h/0xCFCh

Regoffset = 0x4h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv							SE	A	P	VGA	MWIE	ESC	Rsv	M E	IO E
Default value after reset = 0000h															

Bit Number	Mnemonic	Description
Bits 15-9	Rsv	Reserved. These bits are hardwired to '0's. Writes have no effect on them.
Bit 8	SE	SERR# Enable. If this bit is set to a '1', the South Bridge may assert SERR# upon detecting a master or target abort in response to a the South Bridge initiated PCI transaction on behalf of IDE master. If this bit is set to '0', the South Bridge will not assert SERR#.
Bit 7	A	Address/Data stepping enable. This bit is hardwired to a '0'. Writes to it have no effect.
Bit 6	P	PERR# response. Setting this bit to '1' enables parity error detection.
Bit 5	VGA	VGA Palette Snoop enable. This bits is hardwired to a '0'. Writes to it have no effect.
Bit 4	MWIE	Master Write and Invalidate Enable. This bit is hardwired to a '0'. Writes to it have have no effect.
Bit 3	ESC	Enable Special cycles. This bit is hardwired to a '0'. Writes to it have no effect.
Bit 2	Rsv	Reserved.
Bit 1	M E	Mem Enable. This bit is hardwired to a '0'. Writes to it have no effect.
Bit 0	IO E	IO Enable. Setting this bit to a '1' enables access to the IDE IO registers.

PCI CONTROLLERS

9.8.4. SOUTH BRIDGE PCI STATUS REGISTER

SB_Stat1

Access = 0xCF8h/0xCFCh

Regoffset = 0x6h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv	SS	SMA	RTA	Rsv	DT		DPED	FBBC	Rsv						
Default value after reset = 0280h															

Bit Number	Mnemonic	Description
Bit 15	Rsv	Reserved. This bit is hardwired to '0'.
Bit 14	SS	Signalled SERR#. This bit is set to a '1'.
Bit 13	SMA	Signalled Master Abort. This bit is set to a '1' when the West Bridge terminates a PCI transaction initiated on behalf of the IDE master with a master abort. The West Bridge master aborts an IDE master cycle if no target responds to this cycle.
Bit 12	RTA	Received Target Abort. This bit is set to a '1' when a PCI transaction initiated by the West Bridge on behalf of the IDE master is terminated with a target abort. Writing a '1' to this bit will clear it.
Bit 11	Rsv	Reserved. This bit is hardwired to '0'.
Bits 10-9	DT	DEVSEL Timing. These bits are hardwired for medium timing to '01'. Writes to these bits have no effect.
Bit 8	DPED	Data Parity Error Detected. This bit is hardwired to '0'.
Bit 7	FBBC	Fast Back-to-Back Capable. This bit is hardwired to '1'.
Bits 6-0	Rsv	Reserved. These bits are hardwired to '0'.

9.8.5. SOUTH BRIDGE REVISION ID REGISTER

This is the 8-bit read only PCI revision identification register.

<i>SB_R_ID1</i>		Access = 0xCF8h/0xCFCh				Regoffset = 0x8h	
7	6	5	4	3	2	1	0
Rsv							
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-0	Rsv	Reserved. These bits are hardwired to 00h in this stepping of the chip.

PCI CONTROLLERS

9.8.6. SOUTH BRIDGE PROGRAMMING INTERFACE REGISTER

Prog_Int

Access = 0xCF8h/0xCFCh

Regoffset = 0x09h

7	6	5	4	3	2	1	0
Rsv	Rsv						
Default value after reset = 8Ah							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved. This bit is hardwired to '1'. Writes to have no effect on this bit.
Bits 6-4	Rsv	Reserved. These bits are hardwired to '0'. These bits are hardwired to '0'.
Bit 3		This bit is hardwired to '1' indicating that the secondary channel is programmable to be either in legacy or native mode.
Bit 2		This bit selects the operating mode of the secondary channel. (see Table 7-17)
Bit 1		This bit is hardwired to '1' indicating that the primary channel is programmable to be either in legacy or native mode.
Bit 0		This bit selects the operating mode of the primary channel. (see Table 7-18)

Table 9-6. Operating Mode of the Secondary Channel

Bit 2	
0	Channel is in legacy mode. In legacy mode the secondary IDE channel occupies IO addresses 170h-177h and 376h.
1	Channel is in native mode. The address range occupied by the secondary IDE controller in native mode is specified by base address registers 2 and 3.

Table 9-7. Operating Mode of the Primary Channel

Bit 0	
0	Channel is in legacy mode. In legacy mode the Primary IDE channel occupies IO addresses 1F0h-1F7h and 3F6h.
1	Channel is in native mode. The address range occupied by the Primary IDE controller in native mode is specified by base address registers '0' and '1'.

9.8.7. SOUTH BRIDGE SUB-CLASS CODE REGISTER

This register is hardwired to 01h, indicating that this is an IDE controller device.

<i>Sub_Class</i>		Access = 0xCF8h/0xCFCh				Regoffset = 0xAh	
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

PCI CONTROLLERS

9.8.8. SOUTH BRIDGE BASE-CLASS CODE REGISTER

This register is hardwired to 01h, indicating that Function 1 is a mass storage device.

<i>Base_Class</i>				Access = 0xCF8h/0xCFCh		Regoffset = 0xBh	
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

9.8.9. SOUTH BRIDGE LATENCY TIMER CONTROL REGISTER

Lat_T

Access = 0xCF8h/0xCFCh

Regoffset = 0xDh

7	6	5	4	3	2	1	0
Rsv							
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-0	Rsv	Reserved. These bits are hardwired to '0'.

PCI CONTROLLERS

9.8.10. SOUTH BRIDGE HEADER TYPE REGISTER

This register is hardwired to 80h, indicating that the South Bridge is a PCI multi-function device.

Head_T

Access = 0xCF8h/0xCFCh

Regoffset = 0xEh

7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0



9.8.11. SOUTH BRIDGE IDE BASE ADDRESS 0 REGISTER

This 32-bit register contains the base IO address for accessing the primary IDE channel command registers. The base address is meaningful only when the Primary channel is programmed for native mode operation. If programmed for legacy mode operation, the primary channel command registers are decoded at 1F0h IO address.

Base0

Access = 0xCF8h/0xCFCh

Regoffset = 0x10h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BA															
Default value after reset = 00000001h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA														Rsv	MSI
Default value after reset = 00000001h															

Bit Number	Mnemonic	Description
Bits 31-3	BA	Base Address. This field specifies the 8-Byte IO address range where the primary channel command registers are located.
Bit 2		Hardwired to '0' to indicate that this base address occupies 4-Bytes in IO space.
Bit 1	Rsv	Reserved. Hardwired to '0'.
Bit 0	MSI	Memory Space Indicator. This bit is hardwired to '1' to indicate IO space.

PCI CONTROLLERS

9.8.12. SOUTH BRIDGE IDE BASE ADDRESS 1 REGISTER

This 32-bit register contains the base IO address for accessing the primary IDE channel Control registers. The base address is meaningful only when the Primary channel is programmed for native mode operation. If programmed for legacy mode operation, the primary channel control register are decoded at 3F6h.

Base1

Access = 0xCF8h/0xCFCh

Regoffset = 0x14h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BA															
Default value after reset = 00000001h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA														Rsv	MSI
Default value after reset = 00000001h															

Bit Number	Mnemonic	Description
Bits 31-2	BA	Base Address. This field specifies the 4-Byte IO address range where the primary channel command registers are located.
Bit 1	Rsv	Reserved. Hardwired to '0'.
Bit 0	MSI	Memory Space Indicator. This bit is hardwired to '1' to indicate IO space.

9.8.13. SOUTH BRIDGE IDE BASE ADDRESS 2 REGISTER

This 32-bit register contains the base IO address for accessing the secondary IDE channel command registers. The base address is meaningful only when the secondary channel is programmed for native mode operation. If programmed for legacy mode operation, the secondary channel command registers are decoded at 170h IO address.

<i>Base2</i>				Access = 0xCF8h/0xCFCh								Regoffset = 0x18h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BA															
Default value after reset = 00000001h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA														Rsv	MSI
Default value after reset = 00000001h															

Bit Number	Mnemonic	Description
Bits 31-3	BA	Base Address. This field specifies the 8-Byte IO address range where the secondary channel command registers are located.
Bit 2		Hardwired to '0' to indicate that this base address occupies 4-Bytes in IO space.
Bit 1	Rsv	Reserved. Hardwired to '0'.
Bit 0	MSI	Memory Space Indicator. This bit is hardwired to '1' to indicate IO space.

PCI CONTROLLERS

9.8.14. SOUTH BRIDGE IDE BASE ADDRESS 3 REGISTER

This 32-bit register contains the base IO address for accessing the secondary IDE channel Control registers. The base address is meaningful only when the secondary channel is programmed for native mode operation. If programmed for legacy mode operation, the secondary channel control register is decoded at 376h.

<i>Base3</i>								Access = 0xCF8h/0xCFCh								Regoffset = 0x1Ch							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16								
BA																							
Default value after reset = 00000001h																							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
BA														Rsv	MSI		
Default value after reset = 00000001h																	

Bit Number	Mnemonic	Description
Bits 31-2	BA	Base Address. This field specifies the 4-Byte IO address range where the secondary channel command registers are located.
Bit 1	Rsv	Reserved. Hardwired to '0'.
Bit 0	MSI	Memory Space Indicator. This bit is hardwired to '1' to indicate IO space.

9.8.15. SOUTH BRIDGE IDE BASE ADDRESS 4 REGISTER

This 32-bit register contains the base IO address for accessing the bus master control and status register.

Base4

Access = 0xCF8h/0xCFCCh

Regoffset = 0x20h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BA															
Default value after reset = 00000001h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												HW		Rsv	MSI
Default value after reset = 00000001h															

Bit Number	Mnemonic	Description
Bits 31-4	BA	Base Address. This field specifies the 16-bytes IO address range where the Bus master control and status registers are located.
Bits 3-2	HW	Hardwired to '0' to indicate that this base address occupies 16-bytes in IO space.
Bit 1	Rsv	Reserved. Hardwired to '0'.
Bit 0	MSI	Memory space indicator. This bit is hardwired to '1' to indicate IO space.

PCI CONTROLLERS

9.8.16. SOUTH BRIDGE IDE TIMING REGISTER

This 16-bit register contains all the IDE timing information for the Read and Write signals. This register is duplicated with the appropriate offsets for the Primary Master, Slave, Secondary Master or Slave Timings. The offsets are shown in [Table 7-19](#)

Table 9-8. Timing Register Location

Regoffset	Timing Register
040h	Primary Master Timing Control
042h	Primary Slave Timing Control
044h	Secondary Master Timing Control
046h	Secondary Slave Timing Control

IDE_Timing

Access = 0xCF8h/0xCFCh

Regoffset = [Table 7-19](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDSMS		IDRT		IDAT		IPRT			IPAT			ISE	EWP	ERP	EPA
Default value after reset = 7F60h															

Bit Number	Mnemonic	Description
Bits 15-14	IDSMS	IDE DMA Speed Mode Select. These bits, along with bits 29-26, determine the width of the read and write signals during DMA transfers. Refer to Table 7-20 to determine the number of clocks for active and recovery times for the read/write signals. The slower modes are normally used for single word DMA modes and the faster modes are used for double word DMA modes.
Bits 13-12	IDRT	IDE DMA Recovery Time. These bits, along with bits 31-30, determine the duration of the recovery (inactive) time of the read/write signals during DMA transfers. Refer to Table 7-21 to determine the number of clocks for recovery times of the read/write signals. Default is 01h.
Bits 11-10	IDAT	IDE DMA Active Time. These bits, along with bits 31-30, determine the duration of the active time of the read/write signals during DMA transfers. Refer to Table 7-22 to determine the number of clocks for active times of the read/write signals. Default is 01h.
Bits 9-7	IPRT	IDE PIO Recovery Time. These bits determine the duration of the recovery (inactive) time of the read/write signals during PIO data transfers. The transfers to non-data registers of the IDE device will always have a recovery time of 10 clocks. Refer to Table 7-23 to determine the number of clocks for recovery times of the read/write signals.

Bit Number	Mnemonic	Description
Bits 6-4	IPAT	<p>IDE PIO Active Time. These bits determine the duration of the active time of the read/write signals during PIO transfers.</p> <p>The transfers to non-data registers of the IDE device will always have an active time of 10 clocks.</p> <p>Refer to Table 7-24 to determine the number of clocks for active times of the read/write signals:</p> <p>Note that the address setup time is implied. After initial start-up latency, the address setup time is shown in Table 7-25</p>
Bit 3	ISE	<p>IOCHRDY Sampling Enable. This bit when set to 1, enables IOCHRDY sampling of the IDE device, i.e., the active read/write signals will be stretched (when IOCHRDY is low), to extend the cycle, if this bit is set. When set to 0, IOCHRDY is ignored and the read/write signals are deasserted after the specified number of PCI clocks.</p>
Bit 2	EWP	<p>Enable Write Posting. This bit when set to 1, enables posting of data into the FIFO during PIO data write transfers. Note that the non-data writes are never posted.</p>
Bit 1	ERP	<p>Enable Read Prefetch. This bit when set to 1 enables data to be prefetched into the data FIFO during PIO read commands. If set to 0, prefetch is completely disabled.</p>
Bit 0	EPA	<p>Enable Prefetch for ATAPI commands. When set to 1, this bit enables prefetching for ATAPI commands (when A0h is written into the command register - Register offset 07h for the device). When set to 0, prefetching during ATAPI commands is disabled. This is to accommodate non-512 boundary data transfers that are supported by ATAPI devices.</p> <p>Prefetch for the IDE controller is given in Table 7-26.</p>

Table 9-9. DMA Speed Mode Select

Bit 15	Bit 14	DMA Speed Mode
0	0	Fast mode
0	1	Medium fast mode
1	0	Medium slow
1	1	Slow mode

Table 9-10. IDE DMA Recovery Time Settings

		Bits 13-12	Bits 13-12	Bits 13-12	Bits 13-12
Bit 15	Bit 14	00	01	10	11
0	0	1	2	3	4
0	1	5	6	7	8
1	0	9	10	11	12
1	1	14	15	16	20

Table 9-11. IDE DMA Active Time Settings

	Bits 11-10	Bits 11-10	Bits 11-10	Bits 11-10
Bits 15-14	00	01	10	11
00	1	2	3	4
01	5	6	7	8
10	9	10	11	12
11	14	15	16	20

Table 9-12. Recovery R/W Signal Time

Bit 9	Bit 8	Bit 7	PCI Clocks
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	12

Table 9-13. Active R/W Signal Time

Bit 6	Bit 5	Bit 4	PCI Clocks
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	12

Table 9-14. Address Setup Time

Bit 6	Bit 5	Address setup time
0	0	1 clock
0	1	2 clocks
1	X	3 clocks

Table 9-15. Prefetch Encoding

Bit 1	Bit 0	Prefetch
0	X	Completely disabled

Table 9-15. Prefetch Encoding

Bit 1	Bit 0	Prefetch
1	0	Enabled for non-ATAPI commands only
1	1	Enabled for all commands

PCI CONTROLLERS

9.8.17. SOUTH BRIDGE MISCELLANEOUS REGISTER

This register contains miscellaneous informations.

SB_Misc1

Access = 0xCF8h/0xCFCh

Regoffset = 0x48h

7	6	5	4	3	2	1	0
SR	Rsv	Rsv	Rsv	Rsv	Rsv	SID	PID
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	SR	Soft Reset. When set to 1, the IDE controller is reset. It does not affect the timing control register. The FIFOs and the internal state machines are cleared.
Bits 6-2	Rsv	Reserved.
Bit 1	SID	Secondary Interrupt Detect. This bit is set when the secondary interrupt is active. It is cleared by writing a 1 to this bit in the register.
Bit 0	PID	Primary Interrupt Detect. This bit is set when the primary interrupt is active. It is cleared by writing a 1 to this bit in the register.

10. ISA INTERFACE

10.1. INTRODUCTION

The ISA Interface provides access to the peripherals available in the STPC device and to Memory and external devices on the ISA bus.

Control of the ISA bus is by the North Bridge which acts as a bridge between the host CPU bus and the PCI bus. Reads and writes which are initiated by the CPU are subtractively decoded. Reads and writes that target North Bridge internal registers or main memory are routed to those targets, and all other reads and writes are sent to the PCI bus. The cycles for interrupt acknowledge, shutdown, stop grant and halt are also sent to the PCI bus.

The North Bridge also routes PCI reads and writes to cache, main memory and its internal registers. The South Bridge acts as a bridge between the PCI bus and the ISA bus. ISA bus cycles may be initiated by PCI bus cycles, or by an ISA bus card. Additionally, refresh cycles are run periodically by the ISA controller.

The South Bridge will claim all PCI cycles which were initiated outside the South Bridge and not claimed by any other PCI slave. Reads and writes to PCI configuration registers are routed appropriately by the South Bridge's PCI controller. All other PCI operations, including reads and writes to the South Bridge internal registers, are sent to the ISA controller. With the exception of writes to the keyboard controller under certain conditions, a read or write cycle sent to the ISA bus controller will create one or more ISA bus cycles.

Because of the speed difference between ISA bus and PCI bus, and the requirement that PCI cycles be less than a certain number of clocks, PCI cycles which go to the ISA bus will require retries on the PCI bus.

The cycles for interrupt acknowledge, shutdown, stop grant and halt are also sent to the ISA bus controller. These cycles do not create ISA bus cycles, but they use the same state machines for timing and arbitration as reads and writes. ISA bus cycles which are initiated by an ISA bus card are either DMA cycles, in which case the address is supplied by the DMA controller, or ISA bus master cycles, in which case the address is supplied by the card itself.

Every cycle initiated on the ISA bus is tried on the PCI bus. If the cycle is claimed by some PCI target, then data is read from or written to that target. If the PCI cycle is not claimed, and the cycle targets a South Bridge internal register, then that register is read from or written to. Otherwise, the target is expected to be on the ISA bus.

10.2. PCI / ISA CYCLES

10.2.1. PCI TO ISA READ AND WRITE

The PCI transfers data four bytes at a time, with byte enables for each byte. The South Bridge's PCI controller transfers these four bytes and four byte enables to the ISA controller. The ISA controller in turn runs zero to four ISA cycles. For 8-bit targets, the enabled bytes are read or written in order, least significant byte (lowest address) first.

For 16-bit targets, enabled bytes are again read or written in order, but a 16-bit transfer is used when an even byte is enabled and the following odd byte is also enabled.

Eight-bit ISA operations are by default four and a half ISACLK cycles, starting on a falling edge of ISACLK and ending on a rising edge. Sixteen-bit cycles are by default two and a half ISACLK cycles, also starting on a falling edge of ISACLK and ending on a rising clock. An additional clock cycle may be added by setting bit 5 in Index Register 50. Cycles can also be extended by pulling IOCHRDY low.

ISA INTERFACE

10.2.2. PCI TO INTERNAL REGISTER READ AND WRITE

All South Bridge internal registers are 8-bit. If an IO read or write targets an internal register, the target is assumed to be 8-bit wide (that is IOCS16# is ignored). Timing for reads and writes to internal registers is the same as 8-bit cycles on the ISA bus (see [Section 10.2.1.](#)).

If a write targets an internal register of the South Bridge, the data is written to the register and also to the ISA bus. If a read targets an internal register, the internal register is read, the South Bridge drives the ISA data bus with the contents of the register, and a ISA read cycle is done.

Registers that are called index registers in this document are indirectly addressed through a register at IO address 22h. There are two copies of this register, one on the North Bridge and one on the South Bridge.

Writes to IO address 22h go to both copies of the register. Reads from IO address 22h normally come from the North Bridge copy of the register, and do not generate a read cycle on the PCI bus. For test purposes, this behaviour can be changed by setting bit zero of index register 21h. In this case, a read from IO address 22h reads the South Bridge copy of the register, using a PCI read cycle.

After selecting an index register by writing to IO address 22h, that index register is read from or written to at IO address 23h. Some index registers are implemented in the North Bridge alone, some in the South Bridge alone, and some are duplicated and implemented in both. Whether an index register is implemented in the North Bridge, South Bridge or both is indicated in the description of that register in this document.

For index registers that are implemented in the North Bridge alone, writes to IO address 23h write to the register, and reads of IO address 23h read from the register, and no PCI cycles are generated.

For index registers that are implemented in the South Bridge alone, writes to IO address 23h write to the register, and reads of IO address 23h read from the register. In both cases, the data must go over the PCI bus.

For index registers that are implemented in both the North Bridge and the South Bridge, writes to IO address 23h write to both copies of the register, requiring a PCI write cycle. Reads to IO address 23h reads from the North Bridge copy of the register, and generate no PCI cycles. For test purposes, this behaviour can be changed by setting bit zero of index register 21h. In this case, the South Bridge copy of the register is read, using a PCI read cycle.

10.2.3. INTERRUPT ACKNOWLEDGE CYCLE

When an interrupt is requested, the interrupt controller in the South Bridge asserts the CPU's interrupt input. When the CPU services the interrupt, it must first get the interrupt vector from the interrupt controller. The interrupt vector is used to find the interrupt service routine. Also, since each interrupt request input of the interrupt controller has its own interrupt vector, the vector tells where the interrupt request came from.

To get the interrupt vector, the CPU generates two interrupt acknowledge cycles. Both of these cycles read data from the interrupt controller. The data returned by the first is ignored, while the data for the second contains the interrupt vector in bits 0-7. The North Bridge handles both of the cycles identically, converting them to PCI interrupt acknowledge cycles.

Outside of the interrupt controller, the South Bridge handles both cycles identically. The ISA controller converts the PCI cycles into interrupt acknowledge cycles for the interrupt controllers. The INTA# input of the interrupt controller is asserted for four and a half ISA bus clocks, starting on a falling edge of that clock, and during this time data is transferred from the interrupt controller to the ISA controller. This can be extended to five and a half clocks by setting bit 5 in Index Register 50h.

10.2.4. ISA TO PCI READ AND WRITE

ISA initiated cycles are converted to PCI cycles by the ISA controller. The South Bridge pulls IOCHRDY low to extend these cycles until the PCI cycle has completed.

10.2.5. ISA TO PCI BUFFERED READS

ISA reads of host memory can be buffered. This is disabled by default, and can be enabled by setting bit 6 in Index Register 50h. When this bit is set, ISA bus initiated reads of host memory addresses always get their data from a four byte buffer in the ISA controller which is filled on demand. This can reduce the amount of traffic for a block memory read by up to a factor of four.

The buffer is filled or refilled, under the conditions listed below, after the start of a ISA initiated read of a host memory address has been detected by the South Bridge. The South Bridge generates a PCI read of four bytes, with the low two bits of the address set to zero, and the rest of the address set to be the same as the address on the ISA bus address. The requested data will be driven by the South Bridge onto the ISA bus to finish the ISA read cycle.

The buffer will be refilled if the data requested by the current read is not in the buffer. Also, to avoid stale data, the buffer will be refilled for:

- The first host memory read after an ISA bus master gets ownership of the bus,
- The first host memory read after any ISA bus cycle which is not a host memory read,
- Any ISA read of a byte in the buffer which has already been read since the buffer was last filled.

If a host memory read can be fulfilled without refilling the buffer, no PCI cycle is generated.

10.2.6. ISA TO PCI POSTED WRITES

ISA writes to host memory can be posted. This is disabled by default, and can be enabled by setting bit 7 in Index Register 50h. When this bit is set, ISA bus initiated writes to host memory addresses go to a four byte buffer in the ISA controller. No PCI write is generated until the buffer is written to host memory.

The buffer is written to host memory when:

- The buffer gets full,
- or there is a host memory write to a location not in the buffer,
- or a host memory write would overwrite data already in the buffer,
- or there is an ISA cycle which is not a host memory write,
- or the current ISA master gives up ownership of the bus.

If writing the buffer to host memory is triggered by an ISA bus cycle, that cycle is held up by pulling IOCHRDY low until the buffer has been written to host memory.

Note that it is possible for the South Bridge to generate writes with discontinuous byte enables if posted writes are enabled.

10.2.7. ISA TO REGISTER READ AND WRITE

ISA initiated cycles which target South Bridge internal registers will first be tried on the PCI bus. If they are not claimed by a PCI target, then the register will be read or written. Reads and writes to IPC registers will cause the South Bridge to pull IOCHRDY low for at least the number of cycles programmed into Index Register 01h. Reads and writes to the South Bridge registers which are not IPC registers are normally

ISA INTERFACE

disabled. These can be enabled by setting bit 7 of Index Register 51h. Writes to these registers require a longer than standard recovery time of two ISACLK periods.

10.3. XBUS READ AND WRITE

The XBUS is an 8-bit subset of the ISA bus that connects low speed devices on the mother board to the CPU. In particular, the Real Time Clock (RTC), the Keyboard Controller, and the BIOS ROM will usually be connected via the XBUS. For the STPC, the XBUS shares address, data and command lines with the ISA bus. No buffers or transceivers are required to connect the XBUS to the ISA bus. The timing for XBUS cycles is the same as that for eight bit ISA cycles, see above.

10.3.1. REAL TIME CLOCK READ AND WRITE

The Real Time Clock (RTC) is connected to the XBUS. However the RTC is not connected to the command lines of the XBUS. Instead, four input pins of the RTC (CS#, AS, RW#, DS) are controlled directly by the STPC. The MOT pin of the RTC must be tied low. The registers in the RTC are accessed indirectly, by first writing the register number to IO port 70h, and then reading or writing the register at IO port 71h.

The RTC input CS# is connected to the logical OR of the outputs RMRTCCS# and ISAOE#. CS# is the chip select for the RTC, and it will be driven low (active) on any IO read or write to port 70h or port 71h, and also will be driven low by reads or writes to ROM address space.

The RTC input AS is directly connected to the RTCAS output. AS is the address strobe for the RTC, and it is asserted (high) during any IO write to port 70h.

The RTC input RW# is connected to the logical OR of the RTCRW# and ISAOE# outputs. RW# is write pulse for the RTC, and it will be asserted (low) during any IO write to port 71h.

The RTC input DS is connected to the logical OR of the South Bridge outputs RTCDS and ISAOE#. DS is the read pulse for the RTC, and it will be asserted (low) during any IO read of port 71h.

The RTC interrupt output IRQ# is directly connected to the IRQ8 input. There is an internal inverter between the pin IRQ8 and the interrupt controller to maintain compatibility with the PC-AT without requiring additional external glue logic.

10.3.2. KEYBOARD CONTROLLER READ AND WRITE

The keyboard controller is connected to the XBUS. The chip select input of the keyboard controller is connected to the logical OR of the KBCS# and ISAOE# outputs.

Reads and writes to IO addresses 60h, 62h, 64h, 66h, 68h, 6Ah, 6Ch, and 6Eh are taken by the South Bridge to be reads and writes to the keyboard controller. Writes to the keyboard controller may be intercepted by South Bridge for keyboard controller emulation. In this case, neither IOW# or KBCS# will be asserted. For writes to the keyboard controller that are not intercepted, both IOW# and KBCS# will be asserted (low) during the write. Similarly, for any reads from the keyboard controller, both IOR# and KBCS# will be asserted (low) during the read.

10.3.3. BIOS ROM READ AND WRITE

The BIOS ROM is connected to the XBUS. The chip select for the ROM is connected to the logical OR of the RMRTCCS# and ISAOE# outputs.

10.3.4. CPU RESET AND GATE A20

Before the 286 CPU, memory space was limited to 1MB. Some software applications used this characteristic to access data in segment 0 by generating an address above the 1MB. To stay compatible with these applications, when the 286 appeared, the PC motherboards included, via the keyboard controller, a mechanism to enable or disable this pre-286 compatibility. This is done by the 'Gate A20' mechanism. When enabled, the CPU A20 address line is propagated to the memory bus. When disabled, the memory bus A20 line is forced to 0 (8086 compatible).

To be able to reset the CPU, the keyboard controller also includes a pin which is connected to the CPU reset pin (only the CPU is reset, not the chipset or external components).

The STPC doesn't provide external pins to be able to control the gate A20 and CPU reset. These features are controlled internally by the keyboard emulation. Thus, the STPC checks the commands and data sent to the keyboard controller, and when it recognizes the related commands, applies them internally. The keyboard emulation must be on (register STPC_MISC0/bit 3 = 0), else you won't be able to reset the CPU and the A20 line will always be masked. This is done in the default configuration.

Notes; Only the P2 write command (D1h) and the reset pulse command (FEh) are emulated. In particular, the P2 read command (D0h) is not emulated, so the return value is the keyboard controller P2 state.

On the other STPCs, the commands and data are forwarded, so the keyboard controller receives and applies them, the resulting actions are ignored by the STPC, but the keyboard controller A20 state reflects the STPC A20 state.

10.3.4.1. Reset Method

To disable Gate A20 (forcing address bit 20 to low), write D1h to the I/O Port 64h then write xxxx xx0xb to I/O Port 60h.

To enable Gate A20 (forcing address bit 20h to high

The Reset, also known as warm reset, is generated by writing data FEh to I/O port 64h or by writing data DEh to I/O port 64h then writing data xxxxxx0 binary (bit 0 = '0') to I/O port 60h.

Fast host CPU reset only is generated by two methods:

- 1) Whenever the STPC detects a write to Port 64h with data FEh.
- 2) Whenever the STPC detects a write to Port 60h following a D1h data write to Port 64h, bit 0 of the data byte being written at Port 60h is '0'.

The CPU reset is at least 16 host clocks. The write cycle is not forwarded to the keyboard controller.

ISA INTERFACE

10.4. ISA STANDARD REGISTERS

The ISA standard registers correspond to the registers in the peripheral components integrated in the STPC as well as the miscellaneous ports implemented on a ISA motherboard. These registers reside in IO space.

The functions controlled by the ISA registers include the DMA and interrupt control, BIOS and keyboard interface.

10.4.1. DMA 1 CONTROLLER REGISTERS

DMA 1 controls 8-bit DMA transfers.

There are 16 DMA 1 registers. They are as shown in [Table 10-1](#).

Table 10-1. DMA1 Registers

IO address bits 15-0	Reset Value	Register Name	Mnemonic
XXXX XX00 000x 0000	xxxx xxxx	DMA 1 Channel 0 Base and Current Address	DMA1_CBA0
XXXX XX00 000x 0001	xxxx xxxx	DMA 1 Channel 0 Base and Current Count	DMA1_CBC0
XXXX XX00 000x 0010	xxxx xxxx	DMA 1 Channel 1 Base and Current Address	DMA1_CBA1
XXXX XX00 000x 0011	xxxx xxxx	DMA 1 Channel 1 Base and Current Count	DMA1_CBC1
XXXX XX00 000x 0100	xxxx xxxx	DMA 1 Channel 2 Base and Current Address	DMA1_CBA2
XXXX XX00 000x 0101	xxxx xxxx	DMA 1 Channel 2 Base and Current Count	DMA1_CBC2
XXXX XX00 000x 0110	xxxx xxxx	DMA 1 Channel 3 Base and Current Address	DMA1_CBA3
XXXX XX00 000x 0111	xxxx xxxx	DMA 1 Channel 3 Base and Current Count	DMA1_CBC3
XXXX XX00 000x 1000	xxxx 0000	DMA 1 Read Status/Write Command register	DMA1_RSWC
XXXX XX00 000x 1001	1111 xxxx	DMA 1 Request register	DMA1_RR
XXXX XX00 000x 1010	0000 0000	DMA 1 Read Command/Write Single Mask register	DMA1_RCWSM
XXXX XX00 000x 1011	0000 0000	DMA 1 Mode register	DMA1_Mode
XXXX XX00 000x 1100	1111 1111	DMA 1 Set/Clear Byte pointer flip-flop	DMA1_SCBPFF
XXXX XX00 000x 1101	0000 0000	DMA 1 Read Temp register/Master Clear	DMA1_RTMC
XXXX XX00 000x 1110	1111 1111	DMA 1 Clear Mask/Clear all request	DMA1_CMCAR
XXXX XX00 000x 1111	1111 1111	DMA 1 Read/Write all Mask register bits	DMA1_RWMB

Note that the not all bits of the address are used.

Programming notes:

Channel 0 corresponds to the internal DRQ0B, channel 1 to DRQ1B, channel 2 to DRQ2B, and channel 3 corresponds to the internal DRQ3B.

10.4.2. INTERRUPT CONTROLLER 1 REGISTERS

There are two interrupt controller 1 registers. They are as shown in [Table 10-2](#).

Interrupt controller 1 is the master interrupt controller.

Table 10-2. Interrupt Controller 1 Registers

IO address bits 15-0	Reset Value	Register Name	Mnemonic
0000 0000 0010 0000	0000 0000	Interrupt Controller 1 register	IC_1
0000 0000 0010 0001	1111 1111	Interrupt Controller 1 Mask register	IC_1MR

Note that not all bits of the address are used.

Programming notes:

Interrupt controller 1 input IR0 is connected IRQ0, IR1 to IRQ1, IR2 to interrupt out from interrupt controller 2, IR3 to IRQ3, IR4 to IRQ4, IR5 to IRQ5, IR6 to IRQ6, and IR7 to IRQ7.

ISA INTERFACE

10.4.3. INTERVAL TIMER REGISTERS

The Interval Timer comprises three independent counters. Counter 0 is used to generate timer interrupts, counter 1 is used to generate ISA bus refresh, and counter 2 is used to create the speaker tone.

There are 4 Interval Timer registers. They are as shown in [Table 10-3](#).

Table 10-3. Interval Timer Registers

IO address bits 15-0	Reset Value	Register Name	Mnemonic
XXXX XX00 010x xx00	xxxx xxxx	Interval Timer Register Counter 0 Count	IT_0
XXXX XX00 010x xx01	xxxx xxxx	Interval Timer Register Counter 1 Count	IT_1
XXXX XX00 010x xx10	xxxx xxxx	Interval Timer Register Counter 2 Count	IT_2
XXXX XX00 010x xx11	1111 1111	Command Mode register	IT_3

Note that not all bits of the address are decoded.

Programming notes:

All three counters are clocked by 1.193 MHz nominal frequency (OSC/12). Counter 0 and counter 1 gates are always on, counter 2 gate is controlled by writing to Port B (see [Section 10.4.4](#)).

10.4.4. PORT B REGISTER

This is the ISA compatible 8-bit Port B register located at xxxx xxxx 0110 xxx1 IO address (bits 15-0). It has the following meaning:

Port_B				Access = 0061h		Regoffset =	
7	6	5	4	3	2	1	0
PE	IOCHK	T/C 2S	ISA RC	ISA IOCHK	PCE	SE	T/C 2 G
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	PE	Parity Error. This bit is set to a '1' whenever a parity error is detected during system memory read operation. Once set, this bit can be cleared by setting bit 2 of this register to a '1'. Bit 2 should be reset to a '0' to enable recording the next parity error. The parity error generates NMI to the host CPU if NMI is enabled. This bit is read-only.
Bit 6	IOCHK	ISA IOCHK# Enable. This bit is set to a '1' when IOCHK# signal of the ISA bus is asserted. Once set, this bit is cleared by setting bit 3 of this register to a '1'. Bit 3 should be reset to a '0' to enable recording the next IOCHK#. IOCHK# generates NMI to the host CPU if NMI is enabled. This bit is read only.
Bit 5	T/C 2S	ISA T/C 2 State. This bit reflects the output of Timer/Counter 2 without any synchronization. This bit is read only.
Bit 4	ISA RC	ISA Refresh Check. This bit toggles on every rising edge of the REFRESH# signal of the ISA bus. This bit is read only.
Bit 3	ISA IOCHK	ISA IOCHK# Enable. This bit is connected to the asynchronous clear input of the flipflop which records the IOCHK#. It must be set to a '1' to clear the flipflop and then set to a '0' to enable further IOCHK# assertions. This bit is read/write and cleared to a '0' by ISA reset.
Bit 2	PCE	Parity Check Enable. This bit is connected to the asynchronous clear input of the flipflop which records the parity error. It must be set to a '1' to clear the flipflop and then set to a '0' to enable further parity errors. This bit is read/write and cleared to a '0' by ISA reset.
Bit 1	SE	ISA Speaker Enable. This bit is ANDed with the Interval Timer counter 2 OUT signal to drive the Speaker output signal. This bit is read/write and cleared to a '0' by ISA reset.
Bit 0	T/C 2G	T/C 2 Gate. This bit is connected to the gate input of the Interval Timer counter 2. This bit is read/write and cleared to a '0' by ISA reset.

ISA INTERFACE

10.4.5. PORT 70H REGISTER

This 8-bit write-only register contains the NMI enable bit and is located at xxxx xxxx 0111 0xx1 IO address.

Port_70			Access = 0070h				Regoffset =	
7	6	5	4	3	2	1	0	
NMI E	Rsv							
Default value after reset = 80h								

Bit Number	Mnemonic	Description
Bit 7	NMI E	NMI Enable. NMI is asserted on encountering IOCHK# on the ISA bus (Port_B) or SERR# on the PCI bus if this bit is set to a '0'. Setting this bit to a '1' disables NMI generation.
Bit 6-0	Rsv	Reserved. must be written to '0's. Read back is undefined.

Programming notes:

Writing to this address also sets the address register in the Real Time Clock (RTC, not part of the STPC, normally connected via the ISA interface).

10.4.6. INTERRUPT CONTROLLER 2 REGISTERS

Interrupt controller 2 is the slave interrupt controller.

Interrupt controller 2 occupies two register locations. They are as shown in [Table 10-4](#).

Table 10-4. Interrupt Controller 2 Registers

IO address bits 15-0	Reset Value	Register Name	Mnemonic
XXXX XX00 101x xxx0	0000 0000	Interrupt Controller 2 register	IC_2R
XXXX XX00 101x xxx1	1111 1111	Interrupt Controller 2 Mask register	IC_2M

Note that not all address bits are decoded.

Programming notes:

Interrupt controller 2 input IR1 is connected to IRQ9, IR2 to IRQ10, IR3 to IRQ11, IR4 to IRQ12, IR6 to IRQ14, IR7 to IRQ15. IR0 driven by IRQ8 inverted. IR5 is driven by an internally generated floating point error interrupt request.

ISA INTERFACE

10.4.7. DMA CONTROLLER 2 REGISTERS

There are 16 DMA 2 registers. They are as shown in [Table 10-5](#).

Table 10-5. DMA Controller 2 Registers

IO address bits 15-0	Reset Value	Register Name	Mnemonic
XXXX XX00 1100 000x	xxxx xxxx	DMA 2 Channel 0 Base and Current Address	DMA2_CBA0
XXXX XX00 1100 001x	xxxx xxxx	DMA 2 Channel 0 Base and Current Count	DMA2_CBC0
XXXX XX00 1100 010x	xxxx xxxx	DMA 2 Channel 1 Base and Current Address	DMA2_CBA1
XXXX XX00 1100 011x	xxxx xxxx	DMA 2 Channel 1 Base and Current	DMA2_CBC1
XXXX XX00 1100 100x	xxxx xxxx	DMA 2 Channel 2 Base and Current Address	DMA2_CBA2
XXXX XX00 1100 101x	xxxx xxxx	DMA 2 Channel 2 Base and Current	DMA2_CBC2
XXXX XX00 1100 110x	xxxx xxxx	DMA 2 Channel 3 Base and Current Address	DMA2_CBA3
XXXX XX00 1100 111x	xxxx xxxx	DMA 2 Channel 3 Base and Current Count	DMA2_CBC3
XXXX XX00 1101 000x	1111 xxxx	DMA 2 Read Status/Write Command register	DMA2_RSWC
XXXX XX00 1101 001x	0000 0000	DMA 2 Request register	DMA2_RR
XXXX XX00 1101 010x	0000 0000	DMA 2 Read Command/Write Single Mask register	DMA2_RCWSM
XXXX XX00 1101 011x	0000 0000	DMA 2 Mode register	DMA2_Mode
XXXX XX00 1101 100x	1111 1111	DMA 2 Set/Clear Byte pointer flip-flop	DMA2_SCBPFF
XXXX XX00 1101 101x	0000 0000	DMA 2 Read Temporary/Master Clear	DMA2_RTMC
XXXX XX00 1101 110x	1111 1111	DMA 2 Clear Mask/Clear all requests register	DMA2_CMCAR
XXXX XX00 1101 111x	1111 1111	DMA 2 Read/Write all Mask register bits	DMA2_RWMRB

Note that the not all bits of the address are used.

10.4.8. DMA PAGE REGISTERS

The DMA Page registers defines address bits [16-23] for DMA transfers controlled by DMA 1 or DMA 2. Bits [0-15] are generated by the DMA controller, bits [16-23] come from the appropriate page register, and bits 31-24 are all zeroes.

There are 16 DMA page registers. They are as shown in [Table 10-6](#).

Table 10-6. DMA Page Registers

IO address bits 15-0	Reset Value	Register Name	Mnemonic
XXXX XX00 100x 0000	xxxx xxxx	DMA Page Register Port 80h (Reserved)	Port_80
XXXX XX00 100x 0001	xxxx xxxx	DMA Page Register Channel 2	DMA_PRC2
XXXX XX00 100x 0010	xxxx xxxx	DMA Page Register Channel 3	DMA_PRC3
XXXX XX00 100x 0011	xxxx xxxx	DMA Page Register Channel 1	DMA_PRC1
XXXX XX00 100x 0100	xxxx xxxx	DMA Page Register Port 84h (Reserved)	Port_84
XXXX XX00 100x 0101	xxxx xxxx	DMA Page Register Port 85h (Reserved)	Port_85
XXXX XX00 100x 0110	xxxx xxxx	DMA Page Register Port 86h (Reserved)	Port_86
XXXX XX00 100x 0111	xxxx xxxx	DMA Page Register Channel 0	DMA_PRC0
XXXX XX00 100x 1000	xxxx xxxx	DMA Page Register Port 87h (Reserved)	Port_87
XXXX XX00 100x 1001	xxxx xxxx	DMA Page Register Channel 6	DMA_PRC6
XXXX XX00 100x 1010	xxxx xxxx	DMA Page Register Channel 7	DMA_PRC7
XXXX XX00 100x 1011	xxxx xxxx	DMA Page Register Channel 5	DMA_PRC5

Table 10-6. DMA Page Registers

XXXX XX00 1000 1100	xxxx xxxx	DMA Page Register Port 8Bh (Reserved)	Port_8B
XXXX XX00 1000 1101	xxxx xxxx	DMA Page Register Port 8Ch (Reserved)	Port_8C
XXXX XX00 1000 1110	xxxx xxxx	DMA Page Register Port 8Dh (Reserved)	Port_8D
XXXX XX00 1000 1111	xxxx xxxx	DMA Page Register Port 8Eh (Reserved)	Port_8E

ISA INTERFACE

10.5. ISA CONFIGURATION REGISTERS

These registers are addressed through the Address Configuration Index (CI) and Data registers.

10.5.1. MISCELLANEOUS CONTROL REGISTER 0

Misc_Cont0			Access = 0022h/0023h			Regoffset = 050h	
7	6	5	4	3	2	1	0
ISA WPE	ISA RBE	ISA WIC	ISA CFS	KRE	CPU D		
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	ISA WPE	ISA Write Post Enable. If '1', posted writes to host memory by ISA DMA or ISA bus master are enabled.
Bit 6	ISA RBE	ISA Read Buffer Enable. If '1', buffered reads of host memory by ISA DMA or ISA bus master are enabled.
Bit 5	ISA WIC	ISA Wait Insert Control. This bit controls if extra wait state is inserted for slower ISA devices. 0: No extra wait state for ISA cycle 1: One extra wait state for ISA cycle
Bit 4	ISA CFS	ISA Clock Frequency Select. This bit selects the ISA clock frequency. 0: ISA clock is 14.31818 MHz / 2 1: ISA clock is PCICLK / 4
Bit 3	KRE	Keyboard Reset Enable. This bit if set to a '1', keyboard emulation fast gate A20 and fast reset are disabled. The source of warm reset indication is from the keyboard controller and the CPU core will use the gate A20 indication from keyboard controller for its internal A20M# input.
Bits 2-0	CPU D	CPU Deturbo. These three bits define the ratio CPU is held. (see Table 10-7).

Table 10-7. CPU Deturbo

Bit 2	Bit 1	Bit 0	CPU Deturbo
0	0	0	deturbo is disabled.
0	0	1	CPU is held 1/2 of the time.
0	1	0	CPU is held 2/3 of the time.
0	1	1	CPU is held 3/4 of the time.
1	0	0	CPU is held 4/5 of the time.
1	0	1	CPU is held 5/6 of the time.
1	1	0	CPU is held 6/7 of the time.
1	1	1	CPU is held 7/8 of the time.

10.5.2. MISCELLANEOUS CONTROL REGISTER 1

Misc_Cont1

Access = 0022h/0023h

Regoffset = 051h

7	6	5	4	3	2	1	0
IPC W	CLK 24	HCLK D	Rsv	ROM	S E S	S D S	S C S
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	IPC W	IPC Write control. This bit controls the ISA master writes to the IPC register 0: ISA master writes to IPC register disabled 1: ISA master writes to IPC register enabled
Bit 6	CLK 24	CLK24 Disable. This bit controls the output of CLK24. 0: CLK24 generated normally 1: Clock synthesiser for CLK24 is disable (CLK24 will not toggle)
Bit 5	HCLK D	HCLK Disable. This bit controls the generation of HCLK. 0: HCLK generated normally 1: Clock synthesiser for HCLK is disabled (HCLK will not toggle)
Bit 4	Rsv	Reserved.
Bit 3	ROM	ROM Write Protect Enable. This bit, if set to a '1', disables write cycles to ROM BIOS on extended bus. If set to '0', write to extended bus ROM BIOS is allowed. Note: This bit can not disable the write to shadowed BIOS in DRAM since after shadow is enabled, all writes to BIOS should be forwarded to extended bus.
Bit 2	S E S	Segment E Share. This bit controls if E0000h-EFFFFh segment shares the FLASH memory with F0000h-FFFFFh segment. 0: Sharing disabled 1: Sharing enabled
Bit 1	S D S	Segment D Share. This bit controls if D0000h-DFFFFh segment shares the FLASH memory with F0000h-FFFFFh segment. 0: Sharing disabled 1: Sharing enabled
Bit 0	S C S	Segment C Share. This bit controls if C0000h-CFFFFh segment shares the FLASH memory with F0000h-FFFFFh segment. 0: Sharing disabled 1: Sharing enabled

ISA INTERFACE

10.5.3. PIRQ ROUTING CONTROL REGISTER 0

This 8-bit register controls the routing of PCI Interrupt A# to one of the interrupt inputs of the 8259 as follows. It applies to interrupts A# to D#:

PIRQ Routing	Regoffset
PIRQ A	52h
PIRQ B	53h
PIRQ C	54h
PIRQ D	55h

PAR_Cont0

Access = 0022h/0023h

Regoffset = [Table 8-1](#).

7	6	5	4	3	2	1	0
RE	Rsv			RC A			
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	RE	Routing Enable. If set to a '1', this bit enables the routing of PCI interrupt, otherwise the PCI interrupt A# is unconnected.
Bits 6-4	Rsv	Reserved. Writes have no affect. Reads return undefined value.
Bits 3-0	RC A	Routing Control. These bits route the PCI interrupt A# (see Table 10-8)

Table 10-8. Routing Control Encoding

Bit 3	Bit 2	Bit 1	Bit 0	Interrupt A# Route	Note
0	0	0	1	Reserved	1
0	0	0	1	Reserved	1
0	0	1	0	Reserved	1
0	0	1	1	IRQ3	
0	1	0	0	IRQ4	
0	1	0	1	IRQ5	
0	1	1	0	IRQ6	
0	1	1	1	IRQ7	
1	0	0	0	Reserved.	1
1	0	0	1	IRQ9	
1	0	1	0	IRQ10	
1	0	1	1	IRQ11	
1	1	0	0	IRQ12	
1	1	0	1	Reserved.	1
1	1	1	0	IRQ14	
1	1	1	1	IRQ15	

Note 1: Interrupt can not be routed to this level.

10.5.4. INTERRUPT LEVEL CONTROL REGISTER 0

This 8-bit register allows interrupt requests to the lower 8259 to be either level or edge sensitive on an interrupt by interrupt basis overriding the global edge/level control bit of the 8259.

IRQ_Lev_C_0

Access = 0022h/0023h

Regoffset = 056h

7	6	5	4	3	2	1	0
IRQ C					Rsv		
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-3	IRQ C	IRQ Control IRQ[7-3]. If set to a '1', the corresponding interrupt request is treated as a level input, otherwise it is treated as the edge sensitive input (compatible to ISA).
Bits 2-0	Rsv	Reserved. Writes have no affect. Reads return undefined value.

ISA INTERFACE

10.5.5. INTERRUPT LEVEL CONTROL REGISTER 1

This register allows interrupt requests to the upper 8259 to be either level or edge sensitive on an interrupt by interrupt basis overriding the global edge/level control bit of the 8259. This register has the following definition.

IRQ_Lev_C_1

Access = 0022h/0023h

Regoffset = 057h

7	6	5	4	3	2	1	0
IRQ C		Rsv	IRQ C				IPC
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-6	IRQ C	IRQ Control IRQ[15-14]. If set to a '1', the corresponding interrupt request is treated as a level input, otherwise it is treated as the edge sensitive input (compatible with ISA).
Bit 5	Rsv	Reserved. Writes have no affect and the reads return undefined value.
Bits 4-1	IRQ C	IRQ Control IRQ[12-9]. If set to a '1', the corresponding interrupt request is treated as a level input, otherwise it is treated as the edge sensitive input (compatible to ISA).
Bit 0	IPC	This bit controls the ISA refresh cycle. Setting to 0 disables ISA refresh and setting to 1 enables ISA refresh. By setting this bit to 1 enables the toggling the ISA Port B refresh bit (see Section 10.4.4.).

10.5.6. IPC CONFIGURATION REGISTER

This 8-bit register controls the timing of the DMA controllers, and also the number of wait states for writes to registers in the IPC.

IPC_Conf

Access = 0022h/0023h

Regoffset = 001h

7	6	5	4	3	2	1	0
IPC WS		DMA		DMA		DMA M	DMA C
Default value after reset = C0h							

Bit Number	Mnemonic	Description
Bits 7-6	IPC WS	IPC Wait States. These bits specify the number of ISACLK wait states for read or write to IPC register1 (see Table 10-9).
Bits 5-4	DMA	DMA 16-Bit Wait States. These bits specify the number of wait states in 16-bit DMA cycles (see Table 10-10).
Bits 3-2	DMA	DMA 8-Bit Wait States. These bits specify the number of wait states in 8 bit DMA cycle (see Table 10-11).
Bit 1	DMA M	DMA MEMR# Timing. If this bit is set to '1' the DMA controllers will assert MEMR# at the the same time as IOW#. If set to '0' (default), MEMR# will be asserted one clock after IOW#.
Bit 0	DMA C	DMA Clock Select. If this bit is set to '0' (default), the DMA controller clock will be ISACLK divided by two, otherwise the DMA controller clock will be ISACLK.

Table 10-9. IPC Wait States

Bit 7	Bit 6	IPC Wait States
0	0	1
0	1	2
1	0	3
1	1	4 (Default)

Table 10-10. DMA 16-bit Wait States

Bit 5	Bit 4	DMA 16-bit Wait States
0	0	1 (Default)
0	1	2
1	0	3
1	1	4

Table 10-11. DMA 8-bit Wait States

Bit 3	Bit 2	DMA 8-bit Wait States
0	0	1 (Default)
0	1	2
1	0	3
1	1	4

Programming notes:

To read or write to this register, write 01 to index register 22h, and then read or write from data register 23h.

10.5.7. VMI IRQ ROUTING CONTROL REGISTER

This 8-bit register controls the routing of VMI Interrupt to one of the interrupt inputs of the 8259 as follows:

VIR_Conf

Access = 0022h/0023h

Regoffset = 058h

7	6	5	4	3	2	1	0
VMIE	Rsv			VMIC			
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	VMIR	VMI Routing Enable. If set to a '1', this bit enables the routing of VMI interrupt, otherwise the VMI interrupt is unconnected.
Bits 6-4	Rsv	Reserved. Writes have no affect. Reads return undefined value.
Bits 3-0	VMIC	VMI Routing Control. These bits route the VMI interrupt (see Table 10-12).

Table 10-12. VMI Routing Control Encoding

Bit 3	Bit 2	Bit 1	Bit 0	VMI Interrupt Route	Note
0	0	0	1	Reserved	1
0	0	0	1	Reserved	1
0	0	1	0	Reserved	1
0	0	1	1	IRQ3	
0	1	0	0	IRQ4	
0	1	0	1	IRQ5	
0	1	1	0	IRQ6	
0	1	1	1	IRQ7	
1	0	0	0	Reserved.	1
1	0	0	1	IRQ9	
1	0	1	0	IRQ10	
1	0	1	1	IRQ11	
1	1	0	0	IRQ12	
1	1	0	1	Reserved.	1
1	1	1	0	IRQ14	
1	1	1	1	IRQ15	

Note 1: Interrupt can not be routed to this level.

ISA INTERFACE

10.5.8. ISA SYNCHRONISER BYPASS REGISTER

This 8-bit register controls whether or not the signals between the PCI logic and the ISA logic are passed through synchronization logic. This bit would normally be set only when the ISA clock is derived from PCI clock (that is index 50h, bit 4 is set to '1'). Setting this bit will result in a small improvement in ISA performance.

ISA_Sync

Access = 0022h/0023h

Regoffset = 059h

7	6	5	4	3	2	1	0
Rsv							SE
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-1	Rsv	Reserved. Writes have no affect. Reads return undefined value.
Bit 0	SE	Synchronization Enable. 0: Enabled 1: Disabled

11. IDE CONTROLLER

11.1. INTRODUCTION

The IDE (Integrated Drive Electronics) controller provides two IDE channels, primary and secondary, for interfacing with up to four IDE drives. It supports PIO modes 0 to 4 plus DMA modes 0 to 2. The timings are individually programmable for all four IDE devices. Each channel has a four double-word FIFO for data transfers which allows four levels of write posting or read prefetch. Accesses to the 8-bit non-data IDE registers bypass the FIFOs.

For each of the four drives there are three bits in the configuration registers which can selectively enable write posting, read prefetch and ATAPI read prefetch. If read prefetch is enabled, the IDE controller will prefetch data from the drive after the first read has been made. The prefetching will stop after 256 data reads (512 Bytes), which is the normal sector size. If the current command to the drive is ATAPI packet (A0h), or service (A2h), then the read prefetch will be disabled unless ATAPI read prefetch is set.

The two channels of the IDE controller can be individually programmed to operate in either legacy or native mode. In legacy mode, the IDE interrupts are hardwired to INT 14 & 15. In native mode, they both connect to PCI INTA. If legacy mode is selected, INT 14 & 15 will not be available on the ISA bus even if IDE interrupts are disabled. In legacy mode, the primary and secondary channels are hardwired to IO addresses 1F0h-1F7h / 3F6h and 170h-177h / 376h respectively. In native mode the IO addresses are programmed by configuration registers. For information on PIO mode, please refer to the ATAPI Standard.

The IDE controller provides DMA bus master transfer between IDE devices and system memory, with scatter/gather capability. By performing the IDE data transfer as a bus master, the Bus Master Device off-loads the CPU (no programmed IO for data transfer) and improves system performance in multitasking environments.

Before issuing the DMA command, the system software must first create a Physical Region Descriptor (PRD) table in system memory. This table contains a list of pointers and byte counts for each entry. A register in the IDE controller is set to point to this table. The IDE DMA controller will read from system memory during DMA initialization. Each entry in the PRD table is eight bytes long and will have the format below:

IDE CONTROLLER

11.2. PRD TABLE ENTRY

PRD1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EOT	Rsv														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOW															Rsv
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31	OET	This bit set to '1' if it is the last entry in the table
Bits 30-16	Rsv	Reserved
Bit 15-1	NOWS	Number of 16-bit data packets
Bit 0	Rsv	Reserved; This bit must be set to 0

PRD0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MRPAS															
Default value after reset = undefined															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MRPAS															Rsv
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bit 31-1	MRPAS	Memory Physical Address of the first descriptor
Bit0	Rsv	Reserved; This bit must be set to 0

The table must be aligned on a 4 byte boundary and should not cross a 64k boundary.

A memory region also should not cross a 64k boundary neither. An example of a PRD table is shown in [Figure 11-1..](#)

The primary and secondary channels each have a PRD address pointer register.

To save pins, the IDE controller shares pins with the ISA interface. On the IDE data bus, CS1 & CS3 signals are shared with the ISA address bus and keyboard controller/RTC pins. These signals are isolated by external transceiver devices. The ISAOE signal selects whether the pins are in IDE or ISA mode. The

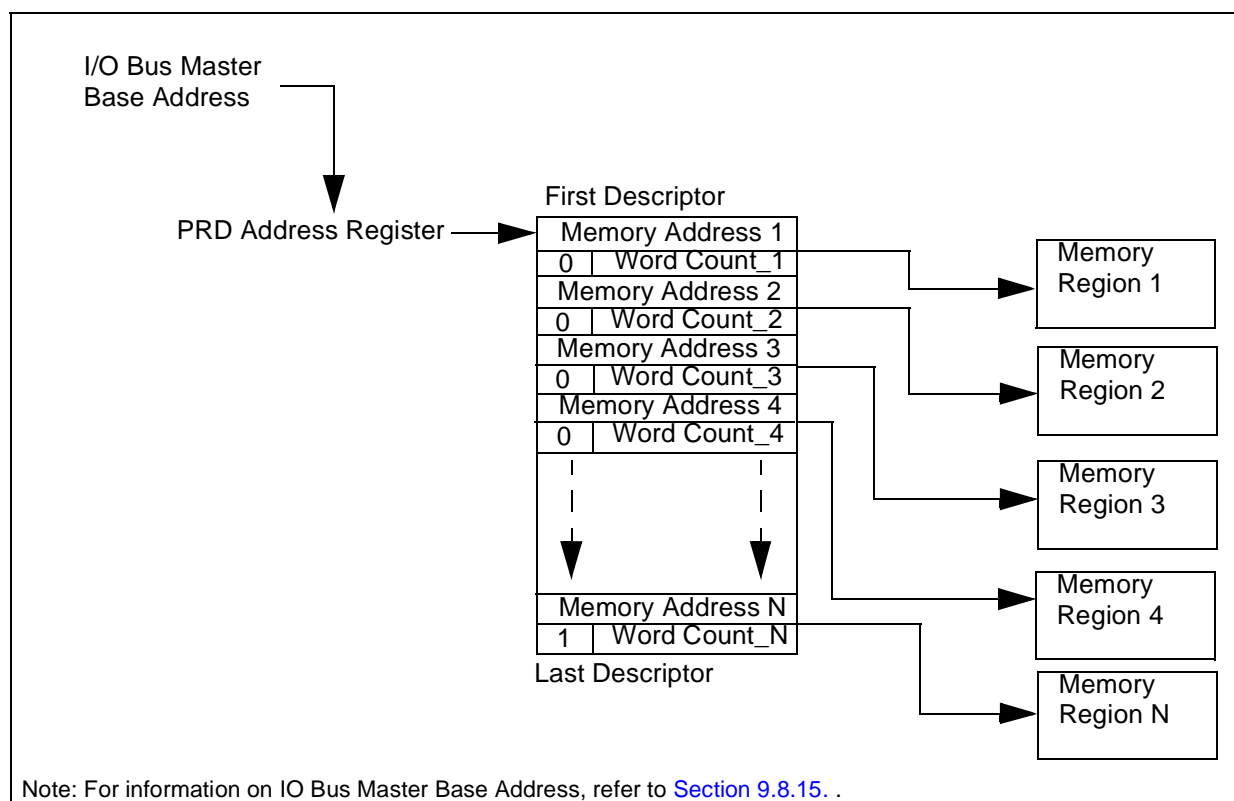


Figure 11-1. PRD Table Entry Example

South Bridge arbitrates between the IDE controller and the ISA bus bridge to select which has control of the shared pins.

11.3. IDE BUS MASTER REGISTERS

This document defines a register level programming interface for the internal busmaster ATA-compatible (IDE) disk controller that directly moves data between IDE devices and main memory.

The system using this programming interface will benefit from bundled software shipped with major Operating Systems, limiting the amount of software development required to provide a complete product.

The master mode programming interface is an extension of the standard IDE programming model. This means that devices can always be dealt with using the standard IDE programming model, with the master mode functionality used when the appropriate driver and devices are present. Master operation is designed to work with any IDE device that supports DMA transfers on the IDE bus. Devices that only work in PIO mode can be used through the standard IDE programming model.

The programming interface defines a simple scatter/gather mechanism, allowing large transfer blocks to be scattered to or gathered from memory. This cuts down the number of interrupts to and interactions with the CPU. The interface defined here supports two IDE channels (primary and secondary). Individual controllers that support more than two channels will need to appear to software as multiple controllers if the standard drivers are to be used. Master IDE controllers should default to Mode 0 Multiword DMA timings to ensure operation with DMA capable IDE devices without the need for controller-specific code to initialize controller-specific timing parameters.

11.3.1. PHYSICAL REGION DESCRIPTOR TABLE

Before the controller starts a master transfer, it is given a pointer to a Physical Region Descriptor Table. This table contains some of a number of the Physical Region Descriptors (PRD); these define the memory areas that are involved in the data transfer. The descriptor table must be aligned on a 4 Byte boundary and the table cannot cross a 64 KByte boundary in memory.

IDE CONTROLLER

11.3.2. PHYSICAL REGION DESCRIPTOR

The physical memory region to be transferred is described by a Physical Region Descriptor (PRD). The data transfer will not proceed until all regions described by the PRDs in the table have been transferred. Each Physical Region Descriptor entry is eight Bytes long.

- The first four bytes specify the byte address of a physical memory region.
- The next two bytes specify the count of the region in bytes (64K byte limit per region).

A value of zero in these two bytes indicates 64 KByte. Bit 7 of the last byte indicates the end of the table; the Bus Master operation terminates when the last descriptor has been retired.

Note: The memory region specified by the descriptor is further restricted such that the region cannot straddle a 64K boundary. This means that the byte count can be limited to 64K, and the incrementer for the current address register need only extend from bit [1] to bit [15]. Also, the total sum of the descriptor byte counts must be equal to, or greater than, the size of the disk transfer request. If greater than, then the driver must terminate the Bus Master transaction (by resetting bit zero of the command register to zero) when the drive issues an interrupt to signal transfer completion.

11.4. BUS MASTER IDE REGISTER DESCRIPTION

The bus master IDE function uses 16 bytes of IO space. All bus master IDE IO space registers can be accessed as byte, word or Dword quantities. The description of the 16 bytes of IO registers is given in [Table 11-5](#).

Table 11-5. Bus Master IDE Register Description

Offset	Register	R/W Status
00h	Bus Master IDE Command register Primary	R/W
01h	Device Specific	
02h	Bus Master IDE Status register Primary	RWC
03h	Device Specific	
04h-07h	Bus Master IDE PRD Table Address Primary	R/W
08h	Bus Master IDE Command register Secondary	R/W
09h	Device Specific	
0Ah	Bus Master IDE Status register Secondary	RWC
0Bh	Device Specific	
0Ch-0Fh	Bus Master IDE PRD Table Address Secondary	R/W

11.6. BUS MASTER IDE COMMAND REGISTER

11.6.1. IDE COMMAND REGISTER

This 8-bit Register is addressed at offset Base + 00h for the Primary IDE Channel and Base + 08h for the Secondary IDE Channel.

This register enables/disables Bus Master capability for the IDE function and provides direction control for the IDE DMA transfers. This register also provides the bits that software uses to indicate DMA capability of the IDE device.

IDE_COM

7	6	5	4	3	2	1	0
Rsv				RWCOM	Rsv		SSBM
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7-4	Rsv	Reserved
Bit 3	RWCOM	<p>Read Write Control. This bit sets the direction of the bus master transfer: when set to zero, PCI bus master reads are performed. When set to one, PCI bus master writes are performed:</p> <p>0 = PCI bus master read 1 = PCI bus master write</p> <p>While a synchronous DMA transfer is in progress, this bit will be READ ONLY. The bit will return to read/write once the synchronous DMA transfer has been completed or halted.</p> <p>This bit must NOT be changed when the bus master function is active</p>
Bit 2-1	Rsv	Reserved
Bits 0	SSBM	<p>Stop/Start Bus Master. Writing a '1' to this bit enables bus master operation of the controller. Bus master operation begins when this bit is detected changing from a zero to a one. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a '0' to this bit. All state information is lost when a '0' is written;. Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (i.e., Bit 0= 1 in the Bus Master IDE Status Register for that IDE channel) and the drive has not yet finished its data transfer (bit 2=0 in the channel's Bus Master IDE Status Register), the Bus Master command is said to be aborted and data transferred from the drive may be discarded before being written to the system memory. This bit is intended to be reset after the data transfer is completed, as indicated by either the Bus Master IDE Active bit or the Interrupt bit of the IDE Status register for that IDE channel being set, or both.</p>

IDE CONTROLLER

11.6.2. IDE STATUS REGISTER

This 8-bit Register is addressed at offset Base + 02h for the Primary IDE Channel and Base + 0Ah for the Secondary IDE Channel.

This register provides status information about the IDE device and state of the IDE DMA transfer. [Table 11-7](#), describes IDE Interrupt Status and Bus Master IDE Active bit states after a DMA transfer has been started.

The IDE Status Register is illustrated in the following table.

IDE_COM

7	6	5	4	3	2	1	0
SO	D1DMA	D0DMA	Rsv		RWI	RWE	RWMI
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	SO	Simplex only. This is hardwired to '0'.
Bit 6	D1DMA	Drive 1 DMA Capable. This read/write bit is set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialised for optimum performance.
Bit 5	D0DMA	Drive 0 DMA Capable. This read/write bit is set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialised for optimum performance.
Bits 4-3	Rsv	Reserved. These bits return '0' when read.
Bit 2	RWI	Read/Write Interrupt. This bit is set by the rising edge of the IDE interrupt line. This bit is cleared when a '1' is written to it by software. Software can use this bit to determine if an IDE device has asserted its interrupt line. When this bit is read as a one, all data transferred from the drive is visible in system memory. For further details see Table 11-7 .
Bit 1	RWE	Read/Write Error. This bit is set when the controller encounters an error in transferring data to/from memory. The exact error condition is bus specific and can be determined in a bus specific manner. This bit is cleared when a '1' is written to it by software.
Bit 0	RWMI	Read/Write Bus Master IDE Active. This bit is set to 1 when bit 0 in the Command register is set to 1. This bit is cleared (set to 0) when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared when the Start bit is cleared in the Command register. When this bit is read as a zero, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted. For further details see Table 11-7 .

Table 11-7. Interrupt/Activity Status Combinations

Bit 2	Bit 0	Description
0	1	DMA transfer is in progress. No interrupt has been generated by the IDE device.
1	0	The IDE device generated an interrupt and the Physical Region Descriptors exhausted. This is normal completion where the size of the physical memory regions is equal to the IDE device transfer size.
1	1	The IDE device generated an interrupt. The controller has not reached the end of the physical memory regions. This is a valid completion case when the size of the physical memory regions is larger than the IDE device transfer size.
0	0	Error condition. If the IDE DMA Error bit is 1, there is a problem transferring data to/from

IDE CONTROLLER

11.7.3. DESCRIPTOR TABLE POINTER REGISTER

This 32-bit Register is addressed at offset Base I/O+ 04h for the Primary IDE Channel and Base I/O+ 0Ch for the Secondary IDE Channel.

This register provides the base memory address of the Descriptor Table. The Descriptor Table must be DWord aligned and must not cross a 4-Kbyte boundary in memory.

DT_Point

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BADT															
Default value after reset = 00h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BADT														Rsv	
Default value after reset = 00h															

Bit Number	Mnemonic	Description
Bits 31-2	BADT	Base address of Descriptor table. This field corresponds to A[31-2].
Bits 1-0	Rsv	Reserved

The Descriptor Table must be Dword aligned. The Descriptor Table must not cross a 64K boundary in memory.

11.8. OPERATION

11.8.1. STANDARD PROGRAMMING SEQUENCE

To initiate a bus master transfer between memory and an Hard Disk device, the following steps are required:

- 1) Software prepares a PRD Table in system memory. Each PRD is 8 bytes long and consists of an address pointer to the starting address and the transfer count of the memory buffer to be transferred. In any given PRD Table, two consecutive PRDs are offset by 8-bytes and are aligned on a 4-byte boundary.
- 2) Software provides the starting address of the PRD Table by loading the PRD Table Pointer Register. The direction of the data transfer is specified by setting the Read/Write Control bit. Clear the Interrupt bit and Error bit in the Status register.
- 3) Software issues the appropriate DMA transfer command to the disk device.
- 4) Engage the bus master function by writing a '1' to the Start bit in the Bus Master IDE Command Register for the appropriate channel.
- 5) The controller transfers data to/from memory responding to DMA requests from the IDE device.
- 6) At the end of the transfer the IDE device signals an interrupt.
- 7) In response to the interrupt, software resets the Start/Stop bit in the command register. It then reads the controller status and then the drive status to determine if the transfer completed successfully.

11.9. DATA SYNCHRONIZATION

When reading data from an IDE device, that data may be buffered by the IDE controller before using a master operation to move the data to memory. The IDE device driver in conjunction with the IDE controller is responsible for guaranteeing that any buffered data is moved into memory before the data is used.

The IDE device driver is required to do a read of the controller Status register after receiving the IDE interrupt. If the Status register returns with the Interrupt bit set, then the driver knows that the IDE device generated the interrupt (important for shared interrupts) and that any buffered data has been flushed to memory. If the Interrupt bit is not set, then the IDE device did not generate the interrupt and the state of the data buffers is unknown.

When the IDE controller detects a rising edge on the IDE device interrupt line (INTRQ), it is required to:

- Flush all buffered data
- Set the Interrupt bit in the controller Status register
- Guarantee that a read to the controller Status register does not complete until all buffered data has been written to memory.

Another way to view this requirement is that the first read to the controller Status register in response to the IDE device interrupt must return with the Interrupt bit set and with the guarantee that all buffered data has been written to memory.

IDE CONTROLLER

11.9.1. STATUS BIT INTERPRETATION

The table below gives a description of how to interpret the Interrupt and Active bits in the Controller status register after a DMA transfer has been started.

Interrupt bit	Active bit	Description:
0	1	DMA transfer is in progress. No interrupt has been generated by the IDE device.
1	0	The IDE device generated an interrupt. The controller exhausted the Physical Region Descriptors. This is the normal completion case where the size of the physical memory regions was equal to the IDE device transfer size.
1	1	The IDE device generated an interrupt. The controller has not reached the end of the physical memory regions. This is a valid completion case where the size of the physical memory regions was larger than the IDE device transfer size.
0	0	This bit combination signals an error condition. If the Error bit in the status register is set, then the controller has some problem transferring data to/from memory. Specifics of the error have to be determined using bus-specific information. If the Error bit is not set, then the PRD's specified a smaller size than the IDE transfer size.

11.10. ERROR CONDITIONS

IDE devices are sector based mass storage devices. The drivers handle errors on a sector by sector basis; either a sector is transferred successfully or it is not. If the IDE DMA slave device never completes the transfer due to a hardware or software error, the Bus Master IDE command will eventually be stopped (by setting Command Start bit to zero) when the driver times out the disk transaction. Information in the IDE device registers will help isolate the cause of the problem.

If the controller encounters an error while doing the bus master transfers, it will stop the transfer (i.e. reset the Active bit in the Command register) and set the ERROR bit in the Status register. The controller does not generate an interrupt when this happens. The device driver can use device specific information (e.g. PCI Configuration Space Status register) to determine what caused the error.

Whenever a requested transfer does not complete properly, information in the IDE device registers (Sector Count) can be used to determine how much of the transfer was completed and to construct a new PRD table to complete the requested operation. In most cases the existing PRD table can be used to complete the operation.

11.11. PCI SPECIFICS

Bus master IDE controllers built to attach to a PCI bus must have the following characteristics:

- 1) The Class Code in PCI configuration space indicates IDE device and bit 7 of the Programming Interface register (offset 0x09) in PCI configuration space must be set to 1 to indicate that the device supports the Master IDE capability.
- 2) The control registers for the controller are allocated via the devices Base Address register at offset 0x20 in PCI configuration space.
- 3) In the controller Status register the Error bit will be set and the Active bit reset if any of the following conditions occur on the PCI bus while the controller is doing a master operation on the bus. The exact cause can be determined by examining the Configuration Space Status register.

Error Condition	Configuration Space Status bits
Target Abort	Any time bit 12 of the Config Space Status register is set.
Master Abort	Any time bit 13 of the Config Space Status register is set.
Data Parity	Any time bit 8 of the Config Space Status register is set.
Error Detected	

12. VGA CONTROLLER

12.1. INTRODUCTION

The STPC integrates a full VGA Controller with Extended Functions together with a Colour Digital to Analog output (RAMDAC) and a Graphics Engine. The VGA Controller provides the basic video display function. It generates the timing and logic required to create an output data stream from the video buffer and the appropriate horizontal and vertical synchronisation pulses.

The on-chip triple RAMDAC runs at up to 135 MHz, using an external frequency synthesiser, allowing a display up to 1280 x 1024 at 75 Hz. Colour is handled using 8-bits, 16-bits, 24-bits or 32-bits per pixel. VDU Graphics standards can be read through the on-chip Display Data Channel (DDC) link.

12.2. VGA CONTROLLER

The VGA controller of the STPC is 100% backward compatible with the VGA standard specification. In addition, enhancements made to the VGA standard are detailed in the following sub-sections.

Resolutions of up to 1024 x 768 and colour depths of 8, 16, 24 and 32 bits per pixel are supported. The integrated RAMDAC supports digital to analog conversion rates up to 135 MHz. This along with peak video bandwidth of 320 MBytes/sec enables the VGA controller to support 1024 x 768 x24 and 800 x 600 x 32 resolutions at 75 Hz refresh rate.

To support vertical resolutions up to 1024 pixels, vertical timing parameters have been extended from 10 bits to 11 bits. The VGA defined horizontal timing parameters are compatible with the above resolutions. The horizontal and vertical timing counters and the sync and blank generation logic operate synchronously to DCLK which can be up to 135 MHz in frequency.

Pixel colour depths are specified by programming the Palette Control register (CR28) appropriately. Eight-bit colour modes use the RAMDAC look-up table to form 18-bit or 24-bit colours. All other modes bypass the look-up table and drive the DACs directly.

The Graphics Core is capable of using up to 4 Mb of available memory as its frame buffer. The Cathode Ray Tube Controller (CRTC) Start Address uses 20-bits to allow for locating the frame buffer at any double word boundary within this 4 Mb of memory. This frame buffer sits within the 16 MBytes Graphics buffer area. Refer to the Graphics Engine Section for further details on the Graphics Memory Architecture.

Video data is automatically extracted from the frame buffer by the CRTC. A FIFO structure ensures that the video display is continually refreshed without loss of data and visual artifacts. Independent high and low level watermarks can be programmed to accelerate or decelerate the demands on the memory arbitration logic.

The CRTC can be programmed to support interlaced monitors and timings. It also supports hardware generated cursor in text mode and a 64 x 64 bit cursor in Graphics modes. This graphics mode cursor is software programmable with separate programmable XOR and AND masks in memory.

If an external add-in VGA card is placed in the system, the on-chip VGA controller can be disabled in order to work with this external card. It is possible to enable / disable the system back to dual use VGA controller if necessary.

VGA CONTROLLER

12.3. VGA REGISTERS

The following sections describe both the standard VGA compatible register definitions and the definitions of register extensions specific to the STPC VGA controller.

The 'X' within some IO addresses represents a 'B' if monochrome operation is enabled and a 'D' if colour operation is in effect.

12.4. GENERAL VGA REGISTERS

12.4.1. MOTHERBOARD ENABLE REGISTER (RW)

MBEN			Access = 0x094h			Regoffset =	
7	6	5	4	3	2	1	0
Rsv		ME	Rsv	MBEN	Rsv		
Default value after reset = 28h							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved, read as '0's.
Bits 5	ME	Motherboard Enable. If the VGA is configured to operate on the motherboard, then when this bit is set to '0', it allows read and write access to port 102h. All other IO and memory accesses are ignored. When set to a '1', this bit allows access to all IO and memory, but access to port 102h is ignored.
Bits 4	Rsv	Reserved, reads as '0'.
Bits 3	MBEN	MBEN Video System Enable. When '0' this bit disables all IO and memory accesses to the VGA as well as the DAC registers. Accesses to 94h remain enabled. When '1', Video system enable bits of port 0102h and 03C3h determine the accessibility of the VGA. The VGA continues to display video data while disabled.
Bits 2-0	Rsv	Reserved, read as '0's.

Programming notes:

The contents of this register are not altered by drawing operations.

12.4.2. ADD-IN VGA ENABLE REGISTER (RW)

ADDEN

Access = 0x46E8h

Regoffset =

7	6	5	4	3	2	1	0
Rsv			AE	ADDEN VSE	Rsv		
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-5	Rsv	Reserved , read as 0's.
Bits 4	AE	Addin Enable . If the VGA is configured to operate on an add-in card, then when this bit is set to '1', it allows read and write access to port 102h. All other IO and memory accesses are ignored. When set to a '0', this bit allows access to IO and memory, but access to port 102h is ignored.
Bits 3	ADDEN VSE	ADDEN Video System Enable . When '0' this bit disables all IO and memory accesses to the VGA as well as the DAC registers. Accesses to 46E8h remain enabled. When '1', Video system enable bits of port 0102h determine the accessibility of the VGA. The VGA continues to display video data while disabled.
2-0	Rsv	Reserved , read as '0's.

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.4.3. VIDEO SUBSYSTEM ENABLE 1 REGISTER (RW)

VSE1				Access = 0x102h			Regoffset =
7	6	5	4	3	2	1	0
Rsv							VSE 1
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-1	Rsv	Reserved, read as '0's.
Bit 0	VSE 1	Video System Enable. When '0', this bit disables all IO and memory accesses to the VGA as well as DAC registers except port 102h. Port 102h remains accessible to allow enabling of the VGA. Ports 46E8h and 94h are also not affected by this bit. The VGA continues to display video data while disabled.

Programming notes:

The contents of this register are not altered by drawing operations.

12.4.4. VIDEO SUBSYSTEM ENABLE 2 REGISTER (RW)

VSE2				Access = 0x3C3h			Regoffset =
7	6	5	4	3	2	1	0
Rsv							VSE 2
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-1	Rsv	Reserved, read as '0's.
Bit 0	VSE 2	Video System Enable. When '0', this bit disables all IO and memory accesses to the VGA as well as DAC registers except ports 102h and 3C3h. Ports 102h and 03C3h remain accessible to allow enabling of the VGA. Port 94h is also not affected by this bit. The VGA continues to display video data while disabled.

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.4.5. MISCELLANEOUS OUTPUT REGISTER (RW)

MISC

Access = 0x3CCCh/0x3C2h

Regoffset =

7	6	5	4	3	2	1	0
VRP	HRP	OEPS	Rsv	CS		E RAM	IO A
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	VRP	Vertical retrace polarity. 0: Active high 1: Active low
Bit 6	HRP	Horizontal retrace polarity. 0: Active high 1: Active low For older IBM compatible colour monitors, the polarity of the vertical and horizontal retrace pulses was used to define the vertical scan rate, as given in Table 12-1 .
Bit 5	OEPS	Odd/Even Page Select. This bit selects between two 64 K pages of memory (of a 128 K plane) when the VGA is in odd/even mode (replaces the least significant bit of the memory address). '0' = low 64 K page. '1' = high 64 K page. This bit is only effective in Mode 0, 1, 2, 3, or 7.
Bit 4	Rsv	Reserved , reads as '0'.
Bits 3-2	CS	Clock Selects. Selects one of the four synthesiser pairs when DCLK source is onchip PLL's.
Bit 1	E RAM	Enable RAM. When '0', this bit disables host accesses to the display RAM. The access to the ROM, however, remains enabled. Setting this bit to '1' enables accesses to the display buffer.
Bit 0	IO A	IO Address. This bit defines the address map of the following registers (see Table 12-2).

Table 12-1. Vertical and Horizontal Polarities

Bit7	Bit6	Active Lines	Vertical Total
0	0	Reserved	Reserved
0	1	400 lines	414 lines
1	0	350 lines	362 lines
1	1	480 lines	496 lines

Table 12-2. IO Address

Register	Bit 0 = '0'	Bit 0 = '1'
CRTC Registers	03BXh	03DXh
Input #1 Register	03BAh	03DAh

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.4.6. INPUT STATUS REGISTER #0 (R)

INP0

Access = 0x3C2h

Regoffset =

7	6	5	4	3	2	1	0
VRF	Rsv		R S	Rsv			
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	VRF	Vertical Retrace Flag. This bit is set at the beginning of the vertical retrace period if bit 4 of CR11 (Vertical Retrace End register) is set to one. Once set, this bit is cleared when bit 4 of CR11 is reset to 0. This recording of the vertical retrace interrupt is independent of bit 5 (disable vertical interrupt) of CR11. See the description of CR11 for more details.
Bits 6-5	Rsv	Reserved. These bits read as ones.
Bit 4	RS	RAMDAC Sense. This bit is connected to the SENSE signal of the RAM-DAC. It is used by the BIOS to auto-detect the monitor type.
Bits 3-0	Rsv	Reserved. These bits read as zero.

12.4.7. INPUT STATUS REGISTER #1 (R)

INP1

Access = 0x3XAh

Regoffset =

7	6	5	4	3	2	1	0
Rsv		DU		VR	Rsv		R
Default value after reset =							

Bit Number	Mnemonic	Description
Bit 7-6	Rsv	Reserved. These bits read as zero.
Bits 5-4	DU	Diagnostic Use. These bits reflect 2 of the 8 bit video output data during display periods and overscan colour data during non-display periods. Selection of one of four pairs of bits is controlled by bits 5-4 of the AR12 as in Table 12-3 .
Bit 3	VR	Vertical Retrace. A one in this position indicates that a vertical retrace is in progress.
Bits 2-1	Rsv	Reserved. Bit 2 reads as one; bit 1 reads as zero.
Bit 0	R	Retrace. A one in this position indicates that a horizontal OR vertical retrace is in progress.

Table 12-3. Video Output Data Selection

AR12		Diagnostic Bits	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	Video2	Video0
0	1	Video5	Video4
1	0	Video3	Video1
1	1	Video7	Video6

VGA CONTROLLER

12.5. VGA SEQUENCER REGISTERS

12.5.1. SEQUENCER INDEX REGISTER (RW)

SRX

Access = 0x03C4h/0x03C5h

Regoffset =

7	6	5	4	3	2	1	0
Rsv					SI		
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved, reads as 0's.
Bit 3		
Bits 2-0	SI	Sequencer Index. These bits point to the register that is accessed by the next read or write to port 03C5h.

Programming notes:

The contents of this register are not altered by drawing operations.

12.5.2. SEQUENCER RESET REGISTER (RW)

SR0

Access = 0x03C4h/0x03C5h

Regoffset = 000h

7	6	5	4	3	2	1	0
Rsv						SR	AR
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-2	Rsv	Reserved , reads as '0's.
Bit 1	SR	Synchronous Reset. When set to '0' terminates display memory accesses. This bit, as well as bit 0 of this register, must be set to '1' to enable sequencer operations. The Clocking Mode register (SR1) bits 0 and 3, and Miscellaneous Output register bits 2-3 must not be changed unless this bit is set to '0' to avoid loss of memory contents.
Bit 0	AR	Asynchronous Reset. This bit performs the same function as bit 1 except when set from '1' to '0', it also clears the Character Map select register (SR3) to '0'.

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.5.3. SEQUENCER CLOCKING MODE REGISTER (RW)

SR1

Access = 0x03C4h/0x03C5h

Regoffset = 001h

7	6	5	4	3	2	1	0
Rsv		SO	S4	DC	SL	Rsv	8/9 DC
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved , reads as '0's.
Bit 5	SO	Screen Off . Setting this bit to '1' blanks the screen by driving black colour (not overscan) on the screen. This facilitates the CPU to access video memory at maximum possible bandwidth.
Bit 4	S4	Shift4 . Together with Shift Load (bit 2), this bit controls the loading of the video serialisers, as in Table 12-4 .
Bit 3	DC	Dot Clk . When '0' sets the dot clock to be the same as the input dot clock. When '1', divides the input dot clock by 2 to derive the dot clock. The input dot clock is divided by 2 for 320 and 360 horizontal pixel modes 0, 1, 4, 5, D and 13. This is can not be used when using an external DCLK
Bit 2	SL	Shift Load , see Bit 4 - Shift4.
Bit 1	Rsv	Reserved , reads as '0'.
Bit 0	8/9 DC	8/9 Dot Clock . When '0', this bit causes the character clock to be 9 dots wide. When '1', an 8-dot wide character clock is selected.

Table 12-4. Video Serialiser Load Clock

Bit4	Bit2	Video Serialiser Load clock	Resolution
0	0	Every character	720 dots/line
0	1	Every second character	360 dots/line
1	X	Every fourth character	180 dots/line

Programming notes:

The contents of this register are not altered by drawing operations.

12.5.4. SEQUENCER PLANE MASK REGISTER (RW)

SR2

Access = 0x03C4h/0x03C5h

Regoffset = 002h

7	6	5	4	3	2	1	0
Rsv				EP3	EP2	EP1	EP0
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved, reads as '0'.
Bit 3	EP3	Enable Plane 3, Write enable for plane 3. A '0' in this bit disables writes to plane 3.
Bit 2	EP2	Enable Plane 2
Bit 1	EP1	Enable Plane 1
Bit 0	EP0	Enable Plane 0

The planes are used in different manners by the various modes. These are shown in [Table 12-5](#).

Table 12-5. Various Modes

Mode	Plane 0	Plane 1	Plane 2	Plane 3
Text Modes 0, 1, 2, 3, 7	Character Data	Attribute Data	Font Data	Unused
16-bit Colour Graphics Modes D, E, 10, 12	Pixel Bit 0	Pixel Bit 1	Pixel Bit 2	Pixel Bit 3
4-Colour Mono Graphics Mode F	Video	Ignored	Intensity	Ignored
4-Colour Modes 4, 5	Even Byte	Odd Byte	Unused	Unused
2-Colour Mono Graphics Mode 6	Even Byte	Odd Byte	Unused	Unused
2-Colour Mono Graphics Mode 11	All Bytes	Unused	Unused	Unused
256-Colour Graphics Mode 13	Byte 0	Byte 1	Byte 2	Byte 3

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.5.5. SEQUENCER CHARACTER MAP REGISTER (RW)

SR3

Access = 0x03C4h/0x03C5h

Regoffset = 003h

5	4	3	2	1	0
SFB	PFB	SFB	SFB	PFB	PFB
Default value after reset = 00h					

Bit Number	Mnemonic	Description
Bit 5	SFB	Secondary Font Block Select bit 0.
Bit 4	PFB	Primary Font Block Select bit 0.
Bit 3	SFB	Secondary Font Block Select bit 2.
Bit 2	SFB	Secondary Font Block Select bit 1.
Bit 1	PFB	Primary Font Block Select bit 2.
Bit 0	PFB	Primary Font Block Select bit 1.

Programming notes:

Used in text mode to select the primary and secondary font tables when the attribute bit 3 is '0' (for primary) or '1' (for secondary) as given in [Table 12-6](#) and [Table 12-7](#).

Table 12-6. Primary Font

Bit 1	Bit 0	Bit 4	Font block #	Table Location
0	0	0	0	0K
0	0	1	4	8 K
0	1	0	1	16 K
0	1	1	5	24 K
1	0	0	2	32 K
1	0	1	6	40 K
1	1	0	3	48 K
1	1	1	7	56 K

Table 12-7. Secondary Font

Bit 3	Bit 2	Bit 5	Font block #	Table Location
0	0	0	0	0 K
0	0	1	4	8 K
0	1	0	1	16 K
0	1	1	5	24 K
1	0	0	2	32 K
1	0	1	6	40 K
1	1	0	3	48 K
1	1	1	7	56 K

This register is reset to '0' by the asynchronous reset via SR0 register.

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.5.6. SEQUENCER MEMORY MODE REGISTER (RW)

SR4

Access = 0x03C4h/0x03C5h

Regoffset = 004h

7	6	5	4	3	2	1	0
Rsv				C4 A	OE	EM	Rsv
Default value after reset = 04h							

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved , reads as '0's.
Bit 3	C4 A	Chain-4 Addressing. When set to '1', this bit forces the two least significant host address bits to select the display buffer plane to be accessed by a host read or write. HA1-0 = '00' selects plane 0, HA1-0 = '01' selects plane 1, etc. For writes, the plane selected by the two address bits still must be enabled via the Plane Mask Register (SR2) in order for the writes to take place. During read transfers, when this bit is set to '1', the Graphics Control Read Map register (GR4) is ignored and the Byte from the plane selected by the two least significant host address bits is returned.
Bit 2	OE	Odd/Even# Addressing. Similar to the Chain-4 bit in that when set to '0' forces the least significant host address bit to select two of the four display planes for host transfers. HA0 = '0' selects planes 0 and 2, and HA1 = '1' selects planes 1 and 3. Selected planes are ANDed with the Plane Mask register (SR2) to generate the plane write enables during write transfers. Read transfers use Map Select bit 1 from GR4 along with HA0 to select one of the 4 Bytes to be returned to the host. Read Map select bit 0 is not used when odd/even addressing mode is enabled.
Bit 1	EM	Extended Memory. When this bit is '0' it indicates 64K of display memory is present. When '1', indicates that 256K of display memory is present.
Bit 0	Rsv	Reserved , reads as '0'.

Programming notes:

The contents of this register are not altered by drawing operations.

12.5.7. EXTENDED REGISTER LOCK/UNLOCK REGISTER (RW)

SR6

Access = 0x03C4h/0x03C5h

Regoffset = 006h

7	6	5	4	3	2	1	0
ER LU							
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-0	ER LU	Extended Registers Lock/Unlock. When written to with 57h, all extended registers are unlocked. When written to with any value other than 57h, all extended registers are locked. When the extended registers are in the locked state, reads to this register return a zero. When the extended registers are in the unlocked state, reads to this register return a '1'.

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.6. GRAPHICS CONTROLLER REGISTERS

12.6.1. GRAPHICS CONTROLLER INDEX REGISTER (RW)

GRX				Access = 0x03CEh/0x03CFh				Regoffset =	
7	6	5	4	3	2	1	0		
Rsv				GCI					
Default value after reset = undefined									

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved, reads as '0's.
Bits 3-0	GCI	Graphics Controller Index. These bits point to the register that is accessed by the next read or write to port 03CFh.

Programming notes:

The contents of this register are not altered by drawing operations.

12.6.2. GRAPHICS SET/RESET REGISTER (RW)

GR0

Access = 0x03CEh/0x03CFh

Regoffset = 000h

7	6	5	4	3	2	1	0
Rsv				GCSR			
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved, reads as '0's.
Bits 3-0	GCSR	Graphics Controller Set/Reset. These bits define the value written to the four memory planes. In Write Mode 0, only the planes enabled by the Enable Set/Reset Register (GR1) are written to. In Write Mode 3, the contents of the Set/Reset register are always enabled. Bit 0 corresponds to memory plane 0, bit 1 to memory plane 1, etc.

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.6.3. GRAPHICS ENABLE SET/RESET REGISTER (RW)

GR1

Access = 0x03CEh/0x03CFh

Regoffset = 001h

7	6	5	4	3	2	1	0
Rsv				GCSR			
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved, reads as '0's.
Bits 3-0	GCSR	Graphics Controller Enable Set/Reset. These bits define which memory planes are to be written to with the value of the corresponding Set/Reset Register (GR0) in Write Mode 0. In Write Mode 3, the Enable Set/Reset register has no affect. Bit 0 corresponds to memory plane 0, bit 1 to memory plane 1, etc.

Programming notes:

The contents of this register are not altered by drawing operations.

12.6.4. GRAPHICS COLOUR COMPARE REGISTER (RW)

GR2

Access = 0x03CEh/0x03CFh

Regoffset = 002h

7	6	5	4	3	2	1	0
Rsv				GCCCR			
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved, reads as '0'.
Bits 3-0	GCCCCR	Graphics Controller Colour Compare Register. These bits are compared with the 4-bit colour of up to 8 pixels in Read Mode 1. The 8-bit (1-bit per pixel) result of the comparison is returned to the host. (A bit of '1' is returned for a match, and '0' for a non-match.) Only those bits enabled by the Colour Don't Care Register (GR7) are matched.

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.6.5. RASTER OP/ROTATE COUNT REGISTER (RW)

GR3

Access = 0x03CEh/0x03CFh

Regoffset = 003h

4	3	2	1	0
GCRO		GCRC		
Default value after reset = undefined				

Bit Number	Mnemonic	Description
Bits 4-3	GCRO	Graphics Controller Raster Op. These bits define the logical operation to apply to the Host data with the data in the Graphics Controller data latch. The possible values of this field are shown in Table 12-8 .
Bits 3-0	GCRC	Graphics Controller Rotate Count. These bits specify the number of bits that the Host data is rotated before the Raster Op is applied. A count of 0 passes the data through unmodified, a count of 1 rotates the Host data 1 bit to the right.

Table 12-8. Raster Operation

Bit 4	Bit 3	Raster Operation
0	0	NOP - Host data passes through unmodified
0	1	Logical AND of Host and latched data
1	0	Logical OR of Host and latched data
1	1	Logical XOR of Host and latched data

Programming notes:

The contents of this register are not altered by drawing operations.

12.6.6. GRAPHICS READ MAP SELECT REGISTER (RW)

GR4

Access = 0x03CEh/0x03CFh

Regoffset = 004h

7	6	5	4	3	2	1	0
Rsv						GCRMS	
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-2	Rsv	Reserved , reads as '0'.
Bits 1-0	GCRMS	Graphics Controller Read Map Select. These bits define the memory plane from which the CPU reads data in Read Mode 0. A value of '00' selects plane 0, '01' selects plane 1, etc. This field also selects one of the 4 Bytes of the Graphics Control Read Data latches.

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.6.7. GRAPHICS MODE REGISTER (RW)

GR5

Access = 0x03CEh/0x03CFh

Regoffset = 005h

7	6	5	4	3	2	1	0
Rsv	SM		OE	RM	Rsv	WM	
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved , reads as '0'.
Bits 6-5	SM	Shift mode These values are given in Table 12-9 .
Bit 4	OE	OddEven . This bit performs no function. It is, however, readable and writable.
Bit 3	RM	Read Mode . If this bit is set to '0', a host read transfer returns the data Byte corresponding to the plane selected by the Read Map Select Register (GR4). This is also called Read Mode 0. When this bit is set to '1', a host read transfer returns the result of the logical comparison between the data in the four planes selected by the Colour Don't Care Register (GR7) and the contents of the Colour Compare Register (GR2). This is also called Read Mode 1.
Bit 2	Rsv	Reserved , reads as '0'.
Bits 1-0	WM	Write Mode . These bits select the write mode as follows in Table 12-10 .

Table 12-9. Shift Register Behaviour

Bit 6	Bit 5	Shift Register Behaviour
1	X	The shift registers are loaded in the manner to support 256 colours. This bit should be set to "1" for mode 13 operation.
0	1	2-bit packed pixel mode (modes 4 and 5) support. The data in the four serial shift registers are formatted as ATR0-3.
0	0	Normal shift mode. M0d7-0, M1d7-0, M2d7-0 and M3d7-0 are shifted out with address to the Attributed Controller.

2-bit packed pixel modes:

ATR0: M1d0 M1d2 M1d4 M1d6 M0d0 M0d2 M0d4 M0d6

ATR1: M1d1 M1d3 M1d5 M1d7 M0d1 M0d3 M0d5 M0d7

ATR2: M3d0 M3d2 M3d4 M3d6 M2d0 M2d2 M2d4 M2d6

ATR3: M3d1 M3d3 M3d5 M3d7 M2d1 M2d3 M2d5 M2d7

Table 12-10. Write Behaviour

Bit 1	Bit 0	Write Behaviour
0	0	Write Mode 0
0	1	Write Mode 1
1	0	Write Mode 2
1	1	Write Mode 3

Where:

Write Mode 0: each of the four display memory planes are written with the host data rotated by the rotate count value specified in GR3.

If the Enable Set/Reset register (GR1) enables any of the four planes, the corresponding plane is written with the data stored in the Set/Reset register (GR0). The raster operation specified in GR3 and the bit mask register (GR8) contents alter data being written.

Write Mode 1: each of the four display memory planes are written with the data from the Graphics Controller read data latches. These latches should be loaded by the host via a previous read. The Raster Operation, Rotate Count, Set/Reset Data, Enable Set/Reset and Bit Mask registers have no effect.

Write Mode 2: memory planes 3-0 are filled with the value of the host data bits 3-0, respectively. Data on the host bus is treated as the colour value. The Bit Mask register (GR8) is effected in this mode. A "1" in a bit position in the Bit Mask register sets the corresponding pixel in the addressed Byte to the colour specified by the host data bus. A "0" set the corresponding pixel in the addressed Byte to the corresponding pixel in the Graphics Controller read latches. The Set/Reset, Enable Set/Reset and Rotate Count register have no effect.

Write Mode 3: each of the four video memory planes is written with 8-bits of the colour value contained in the Set/Reset register for that plane. The Enable Set/Reset register as no effect, all bits are enabled. The host data is rotated and ANDed with the Bit Mask register to form an 8-bit value that performs the same function as the Bit Mask register in Write Modes 0 and 2. This write mode can be used to fill an area with a single colour or pattern.

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.6.8. GRAPHICS MISCELLANEOUS REGISTER (RW)

GR6

Access = 0x03CEh/0x03CFh

Regoffset = 006h

7	6	5	4	3	2	1	0
Rsv				MM		C	GM
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved , read as '0'.
Bits 3-2	MM	Memory Map . These bits specify the map of the display memory buffers in the CPU address space. They are defined as follows in Table 12-11 .
Bit 1	C	Chain2 . This bit performs no function. It is, however, readable and writable.
Bit 0	GM	Graphics Mode . When this bit is set to '1' graphics mode is selected; otherwise when set to '0' alphanumeric mode is selected. This bit is duplicated in AR10[0].

Table 12-11. Address Map

Bit 3	Bit 2	Address Map
0	0	A0000h to BFFFFh (128K)
0	1	A0000h to BFFFFh (128K)
1	0	B0000h to B7FFFh (32K)
1	1	B8000h to BFFFFh (32K)

Programming notes:

The contents of this register are not altered by drawing operations.

12.6.9. GRAPHICS COLOUR DON'T CARE REGISTER (RW)

GR7

Access = 0x03CEh/0x03CFh

Regoffset = 007h

7	6	5	4	3	2	1	0
Rsv				DCPS			
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved, read as '0'.
Bits 3-0	DCPS	Dont_care Colour Plane Selects. One bit per plane determine whether the corresponding colour plane becomes a don't care when a CPU read from the video memory is done in Read Mode 1. A '1' makes the corresponding plane a don't care plane.

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.6.10. GRAPHICS BIT MASK REGISTER (RW)

GR8

Access = 0x03CEh/0x03CFh

Regoffset = 008h

7	6	5	4	3	2	1	0
BM							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	BM	Bit Mask. Any bit programmed to a '0' in this register will cause the corresponding bit in each of the four memory planes to be left unchanged by all operations. The data written into memory in this case will be the data which was read in the previous read operation and stored in the Graphics Controller's read latch. The bit mask is applicable to any data written by the host. The bit mask applies to all four planes simultaneously.

Programming notes:

The contents of this register are not altered by drawing operations.

12.7. ATTRIBUTE CONTROLLER REGISTERS

12.7.1. ATTRIBUTE CONTROLLER INDEX (RW)

The Attribute Controller Index register is used to index into the Attribute Data register array.

Port 3C0h is used for write access to both this index register and, in a subsequent write to this address, to the data register pointed to by the index. There is a flip-flop which changes state after each write to this port. The state of the flip-flop determines whether the next IO write to 3C0h will be to the index register or to a data register. The flip-flop may be initialised - to point to the index register - by performing a read from Input Status Register #1 (IO address 3XAh).

ARX		Access = 0x3C0h					Regoffset =
7	6	5	4	3	2	1	0
Rsv		PAS	ACI				
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved. Must be written as zero.
Bit 5	PAS	Palette Address Source. When set to zero, allows host write access to the Attribute Palette Registers. The CRT display is turned off while this bit stays zero and overscan colour is displayed. Setting this bit to one allows normal video pixel display and disables host write access to the Palette registers.
Bits 4-0	ACI	Attribute Controller Index. Points to the data register which will be accessed by the next write to port 3C0h or the next read from port 3C1h. A sample program could be as follows: <pre> mov DX, 3DAh in AL, DX mov AL, Index mov DX, 3C0h out DX, AL mov AL, Data out DX, AL </pre>

VGA CONTROLLER

12.7.2. ATTRIBUTE PALETTE REGISTERS (RW)

These sixteen registers provide one level of indirection between the colour data stored in the display frame buffer and the displayed colour on the CRT screen. In all modes except 256 colour mode, the (maximum) 4-bit raw colour values select one of these sixteen Palette registers. The 6-bit output of the Palette registers is combined with bits 3-2 of AR14 to form the 8-bit output of the VGA controller. In addition, bits 5-4 of the VGA output may come from either Palette register bits 5-4 or from AR14 bits 1-0 depending on the state of the V54 bit (bit 7) of register AR10.

AR0-ARF

Access = 0x3C1h/0x3C0h

Regoffset =

7	6	5	4	3	2	1	0
Rsv		CV					
Default value after reset =							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved. Must be written as zero.
Bits 5-0	CV	6-bit Colour Value.

12.7.3. ATTRIBUTE CTRL MODE REGISTER (RW)

AR10

Access = 0x3C1h/0x3C0h

Regoffset =

7	6	5	4	3	2	1	0
V54	PW	PPC	Rsv	BE	LGE	MGE	GM
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	V54	V54 Select. This bit determines whether bits 5-4 of the VGA pixel output come from the Video54 field of AR14 (bits 1-0) or from the normal output of the VGA Palette registers. Setting this bit to one selects the Video54 field.
Bit 6	PW	Pixel Width. When this bit is set to one, pixels are clocked at half the normal rate. The effect is to double the width of pixels displayed on the CRT.
Bit 5	PPC	Pixel Panning Compatibility. When VGA split screen is in effect, this bit controls whether both screens or just the top one are affected by Pixel and Byte Panning fields. When set to zero, both screens pan together.
Bit 4	Rsv	Reserved.
Bit 3	BE	Blink Enable. Setting this to one enables blinking in both text and graphics modes. When this bit is set to one in text mode, character attribute bit 7 is used on a character by character basis to enable or disable blinking. When this bit is set to zero in text mode, character attribute bit 7 controls character intensity. The blinking rate is equal to the vertical retrace rate divided by 32 (about twice per second). Setting this bit to one in graphics modes causes the VGA palette input bit 3 to toggle (approx twice per second) if the incoming pixel bit 3 is high.
Bit 2	LGE	Line Graphics Enable. Setting this bit to one forces the ninth pixel of a line graphics character (ascii codes C0h through DFh) to be the same as the eighth pixel. Setting it to zero forces the ninth pixel to be displayed as the background colour. Ninth pixels of all other ascii codes are always displayed as background colour. This bit has no meaning when character width is not set to nine or during graphics modes.
Bit 1	MGE	Mono Attributes Enable. Setting this bit to one in graphics modes while Bit 3 of this register is also one causes the VGA palette input bit 3 to toggle regardless of the incoming pixel's bit 3.
Bit 0	GM	Graphics Mode. Set this bit to one for graphics mode, zero for text mode.

VGA CONTROLLER

12.7.4. ATTRIBUTE CTRL OVERSCAN COLOUR REGISTER (RW)

AR11

Access = 0x3C1h/0x3C0h

Regoffset =

7	6	5	4	3	2	1	0
BC							
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-0	BC	Border Colour. These bits define the colour of the CRT border if there is one. The border or overscan region is that part of the display between where active pixels are displayed and those where the blank signal is active.

12.7.5. ATTRIBUTE COLOUR PLANE ENABLE REGISTER (RW)

AR12

Access = 0x3C1h/0x3C0h

Regoffset =

7	6	5	4	3	2	1	0
Rsv		VSMC		CPE			
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved. These bits should be written as zero.
Bits 5-4	VSMC	Video Status Mux Control. These bits select two of the eight output bits of the Attribute Controller to be read via Input Status Register #1 (3XAh) bits 5-4. The selection is as given in Table 12-12 .
Bits 3-0	CPE	Colour Plane Enable. These four bits are ANDed with the frame buffer data before being input into the Palette. If any of these bits are zero, the corresponding plane from the frame buffer will be masked out of the Palette look up.

Table 12-12. Video Status Mux Control

AR12[5]	AR12[4]	ISR[5]	ISR[4]
0	0	PD[2]	PD[0]
0	1	PD[5]	PD[4]
1	0	PD[3]	PD[1]
1	1	PD[7]	PD[6]

VGA CONTROLLER

12.7.6. ATTRIBUTE HORZ PIXEL PANNING REGISTER (RW)

AR13

Access = 0x3C1h/0x3C0h

Regoffset =

7	6	5	4	3	2	1	0
Rsv				HPP			
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved. These bits should be written as zero.
Bits 3-0	HPP	Horizontal Pixel Panning. These bits specify the number of pixels by which to shift the display left (see Table 12-13).

Table 12-13. Horizontal Pixel Panning

H Pixel Pan	Shift		
	9 pixels/chr	8 pixels/chr	mode 13
0	1 pixel left	0 pixels	0 pixels
1	2 pixels left	1 pixel left	0 pixels
2	3 pixels left	2 pixels left	1 pixel left
3	4 pixels left	3 pixels left	1 pixel left
4	5 pixels left	4 pixels left	2 pixels left
5	6 pixels left	5 pixels left	2 pixels left
6	7 pixels left	6 pixels left	3 pixels left
7	8 pixels left	7 pixels left	3 pixels left
8-15	0 pixels	undefined	undefined

12.7.7. ATTRIBUT COLOUR SELECT REGISTER (RW)

AR14

Access = 0x3C1h/0x3C0h

Regoffset =

7	6	5	4	3	2	1	0
Rsv				V76		V54	
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved. These bits should be written as zero.
Bits 3-2	V76	Video76. In all modes except 256 colour mode (mode 13), these bits are output onto bits 7-6 of the VGA pixel data output port.
Bits 1-0	V54	Video54. When bit 7 of AR10 is set to '1', these bits are output onto bits 5-4 of the VGA pixel data output port.

VGA CONTROLLER

12.8. CRT CONTROLLER REGISTERS

The STPC implements an extension of the VGA CRTC controller. The CRTC controller supports up to 1024 x 768 display resolutions at 75 HZ refresh rates as defined by VESA Monitor Timing Standard. The horizontal timing control fields are all VGA compatible.

The vertical timings are extended by 1-bit to accommodate above display resolution. The address registers are extended to allow locating the frame buffer in anywhere within the first 4 Mb of physical main memory.

12.8.1. INDEX REGISTER (RW)

The CRTC Index register points to an internal register of the CRT controller. The seven least significant bits determine which register will be pointed to in the next register read/write operation to IO port 3B5/3D5.

CRX		Access = 0x3X4h/0x3X5h				Regoffset =	
7	6	5	4	3	2	1	0
Rsv	CRTC I						
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved. Must be written to '0's. Read back is undefined.
Bits 6-0	CRTC I	CRTC Index. Points to the CRTC register that will be accessed by an IO cycle at 03B5h/03D5h.

12.8.2. HORIZONTAL TOTAL REGISTER (RW)

The horizontal total register defines the total number of characters in a horizontal scan line, including the retrace time. The characters displayed on the screen are counted by a character counter. A count of 0 corresponds to the first displayed character at the left side of the screen. The value of the character counter is compared with the value in this register to provide the horizontal timing. A character is composed of 8 or 9 pixels as defined in Sequencer clocking mode register. All horizontal and vertical timing is based on the contents of this register.

The maximum horizontal resolution possible with this field is approximately $260 \times 8 \times 0.8 = 1664$. (260 is $255+5$, 0.8 is the fraction of a horizontal scan period during which active pixels are displayed).

CR0

Access = 0x3X4h/0x3X5h

Regoffset = 000h

7	6	5	4	3	2	1	0
Default value after reset = 00h							

Programming notes:

The 8-bit value in this register = Total number of characters - 5.

VGA CONTROLLER

12.8.3. HORIZ DISPLAY END REGISTER (RW)

This 8-bit read/write register defines the total number of displayed characters in a scan line.

<i>CR1</i>		Access = 0x3X4h/0x3X5h				Regoffset = 001h	
7	6	5	4	3	2	1	0
Default value after reset = undefined							

Programming notes:

The 8-bit value in this register = Total number of displayed characters - 1.

12.8.4. HORIZ BLANKING START REGISTER (RW)

This 8-bit read/write register defines when the horizontal blanking will start. The horizontal blanking signal becomes active when the horizontal character count equals the contents of this register.

CR2

Access = 0x3X4h/0x3X5h

Regoffset = 002h

7	6	5	4	3	2	1	0
Default value after reset = undefined							

VGA CONTROLLER

12.8.5. HORIZ BLANKING END REGISTER (RW)

CR3

Access = 0x3X4h/0x3X5h

Regoffset = 003h

7	6	5	4	3	2	1	0
Rsv	DESC		HBEV				
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved. This readable and writable bit must be written to as '1' to ensure proper VGA operation. It resets to one.
Bits 6-5	DESC	Display Enable Skew Control. These bits delay the display enable by the specified number of character clocks. The result is that the video output stream is delayed by the same amount resulting in wider left border and shrunk right border. This field is in unknown state after reset.
Bits 4-0	HBEV	Horizontal Blanking End Value Bits 4-0. These bits specify the least significant 5-bits of the 6-bit wide Horizontal Blanking End value. The sixth bit is located in CRTC Horizontal Retrace End register. This field is in unknown state after reset.

Programming notes:

This field controls the width of the horizontal blanking signal as follows:

Horizontal Blanking start register + width of the blanking signal = 6-bit Horizontal blanking end value.

The blanking signal set in CR2 and CR3 should start at least 23 GCLKs prior to the start of video window.

12.8.6. HORIZ RETRACE START REGISTER (RW)

This 8-bit register defines the character position at which the horizontal sync becomes active.

CR4

Access = 0x3X4h/0x3X5h

Regoffset = 004h

7	6	5	4	3	2	1	0
Default value after reset = undefined							

VGA CONTROLLER

12.8.7. HORIZONTAL RETRACE END REGISTER (RW)

CR5

Access = 0x3X4h/0x3X5h

Regoffset = 005h

7	6	5	4	3	2	1	0
HBEV	HRSC		HRWV				
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bit 7	HBEV	Horizontal Blanking End Value Bit 6. This is the sixth bit of the Horizontal Blanking end field. Refer to CRTC Horizontal Blanking end register for more details.
Bits 6-5	HRSC	Horizontal Retrace Skew Control. This field delays the start of the horizontal sync by the specified number of character clocks. For text mode operation, this field should be programmed to '1'.
Bits 4-0	HRWV	Horizontal Retrace Width Value. These 5 bits specify the width of the horizontal sync signal as follows: Horizontal Retrace Start register + width of the horizontal sync = 5-bit Horizontal retrace end value.

12.8.8. VERTICAL TOTAL REGISTER (RW)

This register contains the least significant 8 bits of the 11-bit wide Vertical Total value. Next most significant 2 bits are located in CRTC overflow register CR7 and the 11th bit is located in Repaint Control Register 4.

CR6		Access = 0x3X4h/0x3X5h				Regoffset = 006h	
7	6	5	4	3	2	1	0
Default value after reset = undefined							

Programming notes:

The value programmed in this register = Total number of scan lines - 2.

VGA CONTROLLER

12.8.9. OVERFLOW REGISTER (RW)

CR7

Access = 0x3X4h/0x3X5h

Regoffset = 007h

7	6	5	4	3	2	1	0
VR	VD	VT	L	VB	VR	VD	VT
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bit 7	VR	Bit 9 of the 11-bit wide Vertical Retrace start register.
Bit 6	VD	Bit 9 of the 11-bit wide Vertical Display end register.
Bit 5	VT	Bit 9 of the 11-bit wide Vertical Total register.
Bit 4	L	Bit 8 of the 11-bit wide Line compare register.
Bit 3	VB	Bit 8 of the 11-bit wide Vertical Blanking start register.
Bit 2	VR	Bit 8 of the 11-bit wide Vertical Retrace start register.
Bit 1	VD	Bit 8 of the 11-bit wide Vertical Display end register.
Bit 0	VT	Bit 8 of the 11-bit wide Vertical Total register.

12.8.10. SCREEN A PRESET ROW SCAN REGISTER (RW)

CR8

Access = 0x3X4h/0x3X5h

Regoffset = 008h

7	6	5	4	3	2	1	0
Rsv	DS		SS				
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved. Must be written to a '0'. Read back is undefined.
Bits 6-5	DS	Display Shift. This field is added to the memory address generated during the display. As a result, the display shifts left by one, two or three Bytes. For both alphanumeric and graphics modes, this implies a left shift by 8, 16 or 24 pixels respectively. This field is encoded as given in Table 12-14 . When the line compare condition becomes true and pixel panning compatibility bit (AR10 bit 5) is a '1', the outputs of bits 5 and 6 are forced '0' until the start of the next vertical sync pulse.
Bits 4-0	SS	Smooth Scroll. This field can be used to implement smooth vertical scrolling. It specifies the starting row scan count of the character cell after a vertical retrace (assuming the scan lines of a character row are numbered starting with 0). Smooth vertical scrolling can be implemented by setting this register to a value between 1 and the value in CR9. As a result, after a vertical retrace, the display will start from the scan line specified in this field instead of 0. This field is effective only for the top half of the screen (Screen A) if split screen mode is in effect. Each horizontal scan increments the horizontal row scan counter and is reset to 0 when it reaches the character cell height value programmed in CR9. If this field is programmed to a value larger than the character cell height, the row scan counter will count up to 1Fh before rolling over. A '0' in this field means no scrolling.

Table 12-14. Byte Panning

Bit 6	Bit 5	Byte Panning
0	0	0 Byte (display shifts 0 pixels left)
0	1	1 Byte (display shifts 8 pixels left)
1	0	2 Bytes (display shifts 16 pixels left)
1	1	3 Bytes (display shifts 24 pixels left)

VGA CONTROLLER

12.8.11. CHARACTER CELL HEIGHT REGISTER (RW)

CR9

Access = 0x3X4h/0x3X5h

Regoffset = 009h

7	6	5	4	3	2	1	0
SC	LC	VB	SLPR				
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bit 7	SC	Scan Double. When set to a '1', this bit allows a 200-line mode to be displayed on 400 display scan lines by dividing the row scan counter clock by 2 to duplicate each scan line. Thus all row scan address counter based timing (including character height and cursor and underline locations) double, as measured in scan lines, when scan doubling is enabled. Scan doubling only effects the way in which data is displayed; it does not effect display timing. If this bit is set without changing anything else, data currently displayed will appear twice as tall; horizontal and vertical sync, blanking etc., will remain the same.
Bit 6	LC	Bit-9 of the 11 bit wide Line Compare field.
Bit 5	VB	Bit-9 of the 11 bit wide Vertical Blank Start field.
Bits 4-0	SLPR	Scan Lines Per Row. This field specifies the number of scan lines per character row minus one.

12.8.12. CURSOR START REGISTER (RW)

CRA

Access = 0x3X4h/0x3X5h

Regoffset = 00Ah

7	6	5	4	3	2	1	0
Rsv		CDE	CSSL				
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved. Must be written to '0's. Read back is undefined.
Bit 5	CDE	Cursor Display Enable. When set to a '0', this bit enables displaying the cursor. Cursor is displayed only in alphanumeric mode. In graphics mode, the cursor is always disabled and this bit has no effect.
Bits 4-0	CSSL	Cursor Start Scan Line. This field, in conjunction with the Cursor End scan line, defines the shape of the cursor. The hardware cursor is represented as a block of pixels occupying a character position. This field determines the first scan line within the character box that should be filled in (the first scan line is numbered as 0). If the cursor start and end scan line numbers are the same, one scan line wide cursor will be displayed. If starting scan line number is larger than the end, no cursor will be displayed. This is illustrated in Cursor Start and End Registers Figure 12-1 .

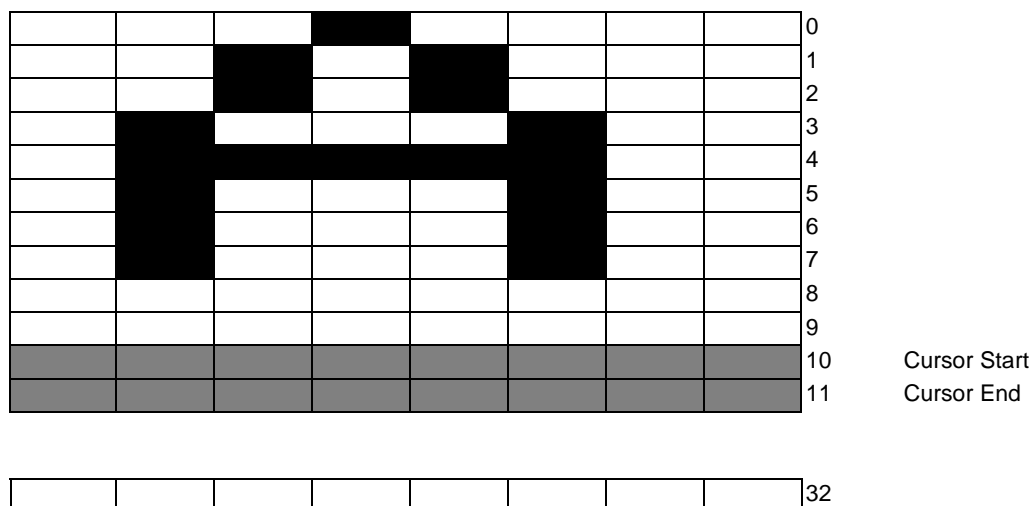


Figure 12-1. Cursor Start and End Registers

VGA CONTROLLER

12.8.13. CURSOR END REGISTER (RW)

CRB

Access = 0x3X4h/0x3X5h

Regoffset = 00Bh

7	6	5	4	3	2	1	0
Rsv	CSC		CESL				
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved. Must be written to '0'. Read back is undefined.
Bits 6-5	CSC	Cursor Skew Control. This field skews the cursor location (defined by the cursor location register) by the specified number of character clocks to the right.
Bit 5	CESL	Cursor End Scan Line. This field, in conjunction with the Cursor Start Scan line field defines the cursor shape. This is illustrated in Figure 12-1 .

12.8.14. START ADDRESS HIGH REGISTER (RW)

This 8-bit register specifies bits 15-8 of the 20-bit display buffer address which will be displayed on the screen after a vertical retrace. Register CRD contains the lower 8-bits and the CRTC extended register CR19 contains the upper 4 bits.

If split screen mode is in effect, this address is the start address of the first of the two (the top one) screens (Screen A). The start address of Screen B (the bottom one) is always 0. The starting scan line for the Screen B is determined by the line compare register (CR18).

CRC		Access = 0x3X4h/0x3X5h				Regoffset = 00Ch	
7	6	5	4	3	2	1	0
Default value after reset =							

VGA CONTROLLER

12.8.15. START ADDRESS LOW REGISTER (RW)

This 8-bit register specifies bits 7-0 of the 20-bit display buffer address which will be displayed on the screen after a vertical retrace. Register CRC contains bits 15-8 and the CRTC extended register CR19 contains the upper 4 bits.

The start address in the CRC, CRD and CRIG does not define the offset within the frame buffer of the 1st displayed pixel but this value divided by 4.

CRD

Access = 0x3X4h/0x3X5h

Regoffset = 00Dh

7	6	5	4	3	2	1	0
Default value after reset =							

12.8.16. TEXT CURSOR OFFSET HIGH REGISTER (RW)

CRE

Access = 0x3X4h/0x3X5h

Regoffset = 00Eh

7	6	5	4	3	2	1	0
CO							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	CO	<p>Cursor offset bits 15-8. This field contains the upper half of the 16-bit cursor offset. The offset is relative to the left-most character on the top of the screen and is specified in terms of character positions. For example, an offset of 0 will place the cursor on the left-most character on the top. An offset of 2 will place the cursor at the third character from the left in the top most row and so on.</p> <p>Since the information is stored in the display memory as character-attribute pairs, the address of the character under the cursor will be exactly twice the cursor offset + the screen base address.</p>

VGA CONTROLLER

12.8.17. TEXT CURSOR OFFSET LOW REGISTER (RW)

This register is the VGA compatible Cursor Offset Low register.

CRF

Access = 0x3X4h/0x3X5h

Regoffset = 00Fh

7	6	5	4	3	2	1	0
CO							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	CO	Cursor offset bits 7-0. This is the lower half of the cursor offset.

12.8.18. VERTICAL RETRACE START REGISTER (RW)

This register contains the lower 8 bits of the 11-bit wide vertical retrace start value. Register CR7 contains bits 8 and 9. Repaint Control Register 4 contains the msb of this 11-bit field. The retrace value is specified in horizontal scan lines where top most scan line on the screen is line 0.

CR10

Access = 0x3X4h/0x3X5h

Regoffset = 010h

7	6	5	4	3	2	1	0
Default value after reset =							

VGA CONTROLLER

12.8.19. VERTICAL RETRACE END REGISTER RW)

CR11

Access = 0x3X4h/0x3X5h

Regoffset = 011h

7	6	5	4	3	2	1	0
CR P	Rsv	VGA IE	VGA IR	VRW			
Default value after reset = 0x10xxxx							

Bit Number	Mnemonic	Description
Bit 7	CR P	CR Protect. This bit when set to a '1', write protects CR0-7 registers except CR7 bit 4.
Bit 6	Rsv	Reserved. This bit is both readable and writable.
Bit 5	VGA IE	VGA Interrupt Enable. When set to a '0', this bit enables the interrupt assertion of the VGA core. Setting this bit to a '1' disables the interrupts.
Bit 4	VGA IR	VGA Interrupt Reset. Setting this bit to a '0', clears the vertical retrace interrupt flip-flop and deasserts the interrupt output (if it was asserted). Setting this bit back to '1' enables the interrupt flip-flop to record the next vertical retrace. The interrupt flip-flop, if enabled by this bit, is set to one scan line after vertical blank is asserted. The flip-flop will not be set and the vertical retrace interrupt will be lost if this bit is set to a '0' when the interrupt occurred. The vertical interrupt flip-flop can be read as bit 7 of Input status register #0.
Bits 3-0	VRW	Vertical Retrace Width. These bits determines the width of the vertical retrace output as follows: Value in the Vertical Retrace Start register (CR10) + Width of the vertical retrace pulse = 4-bit value to be programmed into this field.

12.8.20. VERTICAL DISPLAY END REGISTER (RW)

This register contains the lower 8-bits of the 11-bit wide Vertical display end value which specifies the scan line position where the display on the screen ends. Bits 8 and 9 are specified in CRTC overflow register and the bit-10 in the Repaint Control Register 4.

CR12

Access = 0x3X4h/0x3X5h

Regoffset = 012h

7	6	5	4	3	2	1	0
Default value after reset =							

Programming notes:

The value in this register = Total number of displayed scan lines - 1.

VGA CONTROLLER

12.8.21. OFFSET REGISTER (RW)

This register defines bits 7-0 of the 10-bit wide logical width of the line displayed on the screen. Extended register CR19 contains the upper two bits. The first scan line displayed on the screen, starts at the address specified in registers CRC, CRD and extended register CR19. The starting address of the next scan line is computed as the Byte starting address of the current row + 2*offset.

CR13

Access = 0x3X4h/0x3X5h

Regoffset = 013h

7	6	5	4	3	2	1	0
Default value after reset = undefined							

12.8.22. UNDERLINE LOCATION REGISTER (RW)

CR14

Access = 0x3X4h/0x3X5h

Regoffset = 014h

7	6	5	4	3	2	1	0
Rsv	DWM	C 4	UL				UE
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved. Must be written to a '0'. Read back is undefined.
Bit 6	DWM	Double Word Mode. If this bit is set to a '1', the address generated by the CRTC memory address counter is shifted up two bits to provide the frame buffer address and bits 1-0 of the frame buffer address are driven from CRTC memory address counter bits 13 and 12 respectively. The logical screen width is multiplied by 8 and added to the starting address of the current scan line to compute the starting address of the next scan line.
Bit 5	C 4	Count by 4. Setting this bit to one causes the memory address counter to increment every four character clocks.
Bits 4-1	UL	Underline Location. This field specifies the horizontal row scan of the character cell at which the underlining will occur assuming that top line of the character cell is numbered 0. Underlining occurs in text (alphanumeric) modes only when an attribute value of 'b000i001' binary is detected (where b indicates blink and i indicates intensified).
Bit 0	UE	Underline Enable. Setting this bit to '1' enables underlining.

Programming notes:

Underlining is enabled only in alphanumeric mode and then it is meaningful only for monochrome display (mode 7). For colour modes, the bit 0 of the attribute Byte is interpreted as foreground colour. There is no explicit bit to disable underlining for colour alphanumeric modes. Instead, it is disabled by programming this field to a value larger than the character cell height programmed in CR9.

VGA CONTROLLER

12.8.23. VERTICAL BLANKING START REGISTER (RW)

This register contains the lower 8-bits of the 11-bit scan line valued where the vertical blanking is to begin. The 9th and 10th bits are located in CR7 and CR9 and the 11th bit is located in Repaint Control Register 4.

CR15		Access = 0x3X4h/0x3X5h				Regoffset = 015h	
7	6	5	4	3	2	1	0
Default value after reset = undefined							

12.8.24. VERTICAL BLANKING END REGISTER

This 8-bit register defines the width of the vertical blanking pulse as follows:

CR16		Access = 0x3X4h/0x3X5h				Regoffset = 016h	
7	6	5	4	3	2	1	0
Default value after reset = undefined							

Programming notes:

Start Vertical Blank value + width of the blanking pulse = Value programmed in this register.

While the register is 8-bits wide, and all bits are readable/writable, only the least significant 7 bits are used in the generation of the vertical pulse.

VGA CONTROLLER

12.8.25. MODE REGISTER (RW)

CR17

Access = 0x3X4h/0x3X5h

Regoffset = 017h

7	6	5	4	3	2	1	0
H V RE	B WM	VGA MAS	Rsv	C 2	DVT	MS	MS
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	H V RE	H/V Retrace Enable. A '0' in this bit position disables the horizontal and vertical retraces and a '1' enables them.
Bit 6	B WM	Byte/Word# Mode. A '1' value in this bit position selects the Byte mode and a '0' selects the word mode. Table 12-15 lists the memory address generation for Byte, word and double-word addressing modes. iA24-0 refer to the output of the internal memory address counter and the memory address is the address presented to the address lines of a 4-Byte wide display buffer memory, that is, each memory address selects 4-Bytes.
Bit 5	VGA MAS	VGA Memory Address Size. When set to a '0', this bit, in Word addressing mode (see above) propagates bit iA13 on the least significant memory address bit. If set to a '1', it propagates bit iA15 instead. iA13 should be used if total display buffer memory is 64K and iA15 should be used if total memory is 256K. It is expected that the VGA Controller will always be used with 256K or larger memory. Therefore this bit should be programmed to a '1'.
Bit 4	Rsv	Reserved. Must be written to a '0'. Read back is undefined.
Bit 3	C 2	Count by 2. Setting this bit to one causes the memory address counter to increment every second character clock.
Bit 2	DVT	Double Vertical Total. This bit when set to '1', causes all the vertical timing counters to operate at half the horizontal retrace rate. The result is that the vertical resolution doubles. The Vertical Total, Vertical Retrace Start, Vertical Display End, Vertical Blanking Start and Line Compare registers can be programmed at half their normal value if this bit is set to a '1'. The vertical timing counters operate at their normal frequency if this bit is set to a '0'.
Bit 1	MS	Memory Segmentation Bit 14. If set to a '0', the row scan counter bit 1 is substituted for memory address bit 14 during display refresh. This has the affect of segmenting the address space such that every other scan line pair is 8K apart. In combination with bit 0, this bit can segment the address space in 4-banks. No such substitution takes place if this bit is set to a '1'.
Bit 0	MS	Memory Segmentation Bit 13. This bit is similar to Bit 1 above in that when set to a '0', row scan counter bit 0 is substituted for display memory address bit 13 during active display time. No such substitution takes place if this bit is set to a '1'.

Table 12-15. Memory Address Generation

Internal Memory Address counter	Byte Mode	Word Mode	Double Word Mode
iA24	iA24	iA23	iA22
iA23	iA23	iA22	iA21
:	:	:	:
:	:	:	:
iA3	iA3	iA2	iA1
iA2	iA2	iA1	iA0
iA1	iA1	iA0	iA13
iA0	iA0	iA13/iA15	iA12

The least significant memory address bit in Word mode is selected between iA13 and iA15 based on bit 5 of this register.

This bit is ignored if Double-word mode bit in CR14 is set to a '1'.

VGA CONTROLLER

12.8.26. LINE COMPARE REGISTER (RW)

This register contains the lower 8 bits of the 10-bit wide Line Compare field. The 9th and 10th bits of this field are held in CR7 and CR9 registers respectively. When the horizontal scan line counter value is equal to the contents of the Line Compare register, the memory address generator and the character row scan count are cleared. As a result the display is split into the two halves. The top half, Screen A displays the contents of the display buffer starting from Start address (CRC and CRD registers) while the bottom half, Screen B, displays the contents of the display buffer starting from address 0.

CR18		Access = 0x3X4h/0x3X5h				Regoffset = 018h	
7	6	5	4	3	2	1	0
Default value after reset = undefined							

Programming Notes

Screen A can be smooth scrolled vertically but Screen B can not. Control is provided via bit 5 of AR10 register to allow Screen B to pan horizontally with Screen A or not.

Split screen function can be disabled by programming the Line compare field to a value larger, typically 3FFh, than the Vertical Total field. This field must be programmed to 3FFh for optimal system performance in native display modes.

12.8.27. GRAPHICS CONTROL DATA (R)

CR22

Access = 0x3X4h/0x3X5h

Regoffset = 022h

7	6	5	4	3	2	1	0
GCDL N							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	GCDL N	Graphics Controller Data Latch N. These bits, when read, provide the state of one of the 4 Graphics Controller's Data Latches. The Graphics Controller Read Map Select register (GR4) specify which latch is read.

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.8.28. ATTRIBUTE ADDRESS FLIP-FLOP (R)

CR24

Access = 0x3X4h/0x3X5h

Regoffset = 024h

7	6	5	4	3	2	1	0
AF	Rsv						
Default value after reset =							

Bit Number	Mnemonic	Description
Bit 7	AF	Attribute flip-flop. This read-only bit indicates the state of the Attribute Controller index flip-flop. When this bit is zero, the next access to IO port 3C0h will be to the Attribute Index register. When this bit is one, the next access will be to an Attribute data register.
Bits 6-0	Rsv	Reserved. Read as zero.

12.8.29. ATTRIBUTE INDEX READBCK (R)

CR26

Access = 0x3X4h/0x3X5h

Regoffset = 026h

7	6	5	4	3	2	1	0
Rsv		PAS	ACI				
Default value after reset =							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved. Read as zero.
Bit 5	PAS	Palette Address Source. This is a read-only copy of Attribute Controller Index register (ARX) bit 5.
Bits 4-0	ACI	Attribute Controller Index. This is a read-only copy of bits 4-0 of the Attribute Controller Index register.

VGA CONTROLLER

12.9. VGA EXTENDED REGISTERS

The following registers are additions to those found in the standard VGA specification. They can only be accessed after register SR6 has been written to with 57h.

A typical sequence in 80X86 assembly could be:

```
max      DX, 3C4h
mov      OX, 5706h
out      DX, AX
```

12.9.1. REPAINT CONTROL REGISTER 0 (RW)

CR19

Access = 0x3X4h/0x3X5h

Regoffset = 019h

7	6	5	4	3	2	1	0
Rsv		CRTC O		CRTC SAF			
Default value after reset =00h							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved. Must be written to '0'.
Bits 5-4	CRTC O	CRTC Offset register Bits 9-8. See CRTC register 13 for details.
Bits 3-0	CRTC SAF	CRTC Start Address Field Bits 19-16. See CRTC register C, D for explanation of the Start Address.

12.9.2. REPAINT CONTROL REGISTER 1 (RW)

CR1A

Access = 0x3X4h/0x3X5h

Regoffset = 01Ah

7	6	5	4	3	2	1	0
HTD	VTD	Rsv	CTM	Rsv	LCE	SBP	VGA AW
Default value after reset = 3Fh							

Bit Number	Mnemonic	Description
Bit 7	HTD	Hsync Toggle Disable. When set to a '1', this bit forces the Hsync to inactive state (high or low as programmed in the bit 6 of the Miscellaneous output register). See note below.
Bit 6	VTD	Vsync Toggle Disable. When set to a '1', this bit forces the Vsync to inactive state (high or low as programmed in the bit 7 of the Miscellaneous output register). See note below.
Bit 5	Rsv	Reserved. This bit always reads as a one.
Bit 4	CTM	Compatible Text Mode. When this bit is set to one, the CRT controller expects the font data format within the frame buffer to be identical to that used by the standard VGA chip. Setting this bit to zero enables "Enhanced Text Mode" as described under CR1C bit 7. Note, though that this bit has the opposite sense of CR1C bit 7.
Bit 3	Rsv	Reserved. This bit always reads as a one.
Bit 2	LCE	Line Compare Enable. Set this bit to zero for 1280x1024 mode and one for all others.
Bit 1	SBP	Six Bit Palette. Set this bit to one to enable VGA compatible 6 bit palette functionality and zero to enable the 8-bit palette.
Bit 0	VGA AW	VGA Address Wrap. Setting this bit to one enables VGA compatible address wrapping such that the CRTC will only address 256kb of frame buffer memory (address bits 16 and above are zeroed). Set this bit to zero for SVGA modes. This bit has no effect on CPU reads or writes to the frame buffer - only CRTC accesses.

Programming notes:

Note: Vertical / Horizontal Synch not toggling is defined by the VESA specification for Monitor Power Down State.

VGA CONTROLLER

12.9.3. REPAINT CONTROL REGISTER 2 (RW)

CR1B

Access = 0x3X4h/0x3X5h

Regoffset = 01Bh

7	6	5	4	3	2	1	0
FIFO LWM					Rsv	V FIFO U	W FIFO U
Default value after reset = 20h							

Bit Number	Mnemonic	Description
Bits 7-3	FIFO LWM	FIFO Low Water Mark. When the FIFO occupancy falls below twice this value, the CRTC will restart frame buffer read cycles to refill the FIFO. This field should only ever be set by the BIOS during mode switches. Setting this field too small results in random pixels being displayed to the screen; setting it too large results in decreased CPU - SDRAM bandwidth. Also, do not set this register to a value greater than that programmed into the high water mark (register CR27).
Bit 2	Rsv	Reserved. This bit is not writable. It reads as zeroes.
Bit 1	V FIFO U	Video FIFO Underflow. This read-only bit is set to one when the video refresh FIFO underflows. As with bit 0, writes to this register clear this bit to zero.
Bit 0	W FIFO U	Warning: FIFO Underflow. This read-only bit is set to one when the CRTC refresh FIFO underflows (the memory subsystem did not keep up with pixel requests. Sampling this bit as a one means that a serious problem exists and the low water mark above should be incremented. Writes to this register (presumably with a larger low water mark value) reset this bit to zero.

12.9.4. REPAINT CONTROL REGISTER 3 (RW)

CR1C

Access = 0x3X4h/0x3X5h

Regoffset = 01Ch

7	6	5	4	3	2	1	0
ETFL	Rsv		Rsv		SC	PSC	EOP
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	ETFL	<p>Enhanced Text Font Load. This bit should be set to one prior to loading fonts for 132 column high speed text mode. It warps the frame buffer addresses such that what appear to be standard text font writes actually get stored into frame buffer plane 2 in a more optimised manner. Specifically, frame buffer address bits 15-5 are swapped down to become bits 10-0 and bits 4-0 are moved up to become bits 15-11.</p> <p>The sequence of events to load 132 column enhanced text fonts is as follows. First, Odd-Even and Chain 4 modes should be turned off, then this bit should be set to one. Fonts should then be loaded in the normal VGA manner and finally this bit should be reset to zero and Text/Odd-Even mode entered.</p> <p>Note that the corresponding address warp for the CRT Controller is performed during font table look-ups when bit 4 of CR1A is set to zero.</p>
Bits 6-5	Rsv	Reserved , read as '0's.
Bits 4-3	Rsv	Reserved . These bits read as '0's.
Bit 2	SC	<p>Sequential Chain-4. When this bit is set to '1', allows the display buffer memory to appear as a normal memory with a Byte address in the host address space mapping into a Byte address in the display buffer address space. Chain-4 in SR4 must be set for Sequential Chain-4 to work</p>
Bit 1	PSC	<p>Page Select Control. This bit provides control over whether the cycle type is read or write, or the upper address bit controls the page selection. The VGA implements two 7-bit page registers, Page 0 and Page 1, to allow mapping the VGA address space anywhere in the 4 MB address space.</p> <p>If this bit is '1', the page selection is based on bit 15 or 16 of host address and the Memory Map bits of Register GR6 in Section 12.6.8, as given in Table 12-16.</p>
Bit 0	EOP	<p>Enable Overlapped Paging. This bit should be turned on to solve the broken line problem. When software wants to draw a line that crosses the current page boundary it turns this bit on to form a page out of half of the current page and half of the next page. Since the hardware adds half page to the address when this bit is on, the software should subtract half page for passing on the address.</p> <p>When this bit is '1', the memory address bits MA17 and MA18 are changed as follows for Normal, Odd/Even and Chain-4 cases, see as given in Table 12-17.</p> <p>For Sequential Chain-4, MA16 and MA15 are changed as given in Table 12-18.</p>

Table 12-16. Page Select

GR6 in Section 12.6.8.			Page Selection
Bit3	Bit2	Size	
0	0	128K	HA16=0 → Page 0; HA16=1 → Page 1
0	1	64K	HA15=0 → Page 0; HA15=1 → Page 1
1	0	32K	Not allowed
1	1	32K	Not allowed

Table 12-17. Enable Overlapped Paging

GR6 Section 12.6.8.			Added to MA18	Added to MA17
Bit3	Bit2	Size		
0	0	128K	1 (256K added)	0
0	1	64K	0	1 (128K added)
1	0	32K	Not allowed	
1	1	32K	Not allowed	

Table 12-18. Sequential Chain-4

GR6 Section 12.6.8.			Added to MA16	Added to MA15
Bit3	Bit2	Size		
0	0	128K	1 (64K added)	0
0	1	64K	0	1 (32K added)
1	0	32K	Not allowed	
1	1	32K	Not allowed	

Programming notes:

The contents of this register are not altered by drawing operations.

12.9.5. PAGE REGISTER 0 (RW)

CR1D

Access = 0x3X4h/0x3X5h

Regoffset = 01Dh

7	6	5	4	3	2	1	0
Rsv	P 0						
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved, read as '0'.
Bits 6-0	P 0	Page 0 Bits 6-0. 7-bit Page register 0 is used to extend the host address to allow the VGA buffer to be located anywhere in the 4 MB frame buffer space. The pages are located on 32K boundaries for Normal, Odd/Even and Chain-4 modes and on 8K boundaries for Sequential Chain-4 mode. This is illustrated in Figure 12-2 .

Programming notes:

Register = A000h mapped to the frame buffer and can be either 8 KBytes or 32 KBytes.

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.9.6. PAGE REGISTER 1 (RW)

CR1E

Access = 0x3X4h/0x3X5h

Regoffset = 01Eh

7	6	5	4	3	2	1	0
Rsv	P 1						
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved, read as '0'.
Bits 6-0	P 1	Page 1 Bits 6-0. 7-bit Page register 1 is used to extend the host address to allow the VGA to be located anywhere in the 4 MB frame buffer space. The pages are located on 32K boundaries for Normal, Odd/Even and Chain-4 modes and on 8K boundaries for Sequential Chain-4 mode. This is illustrated in Figure 12-2 .

Programming notes:

Register = A800h mapped to the frame buffer and can be either 8 KBytes or 32 KBytes.

The contents of this register are not altered by drawing operations.

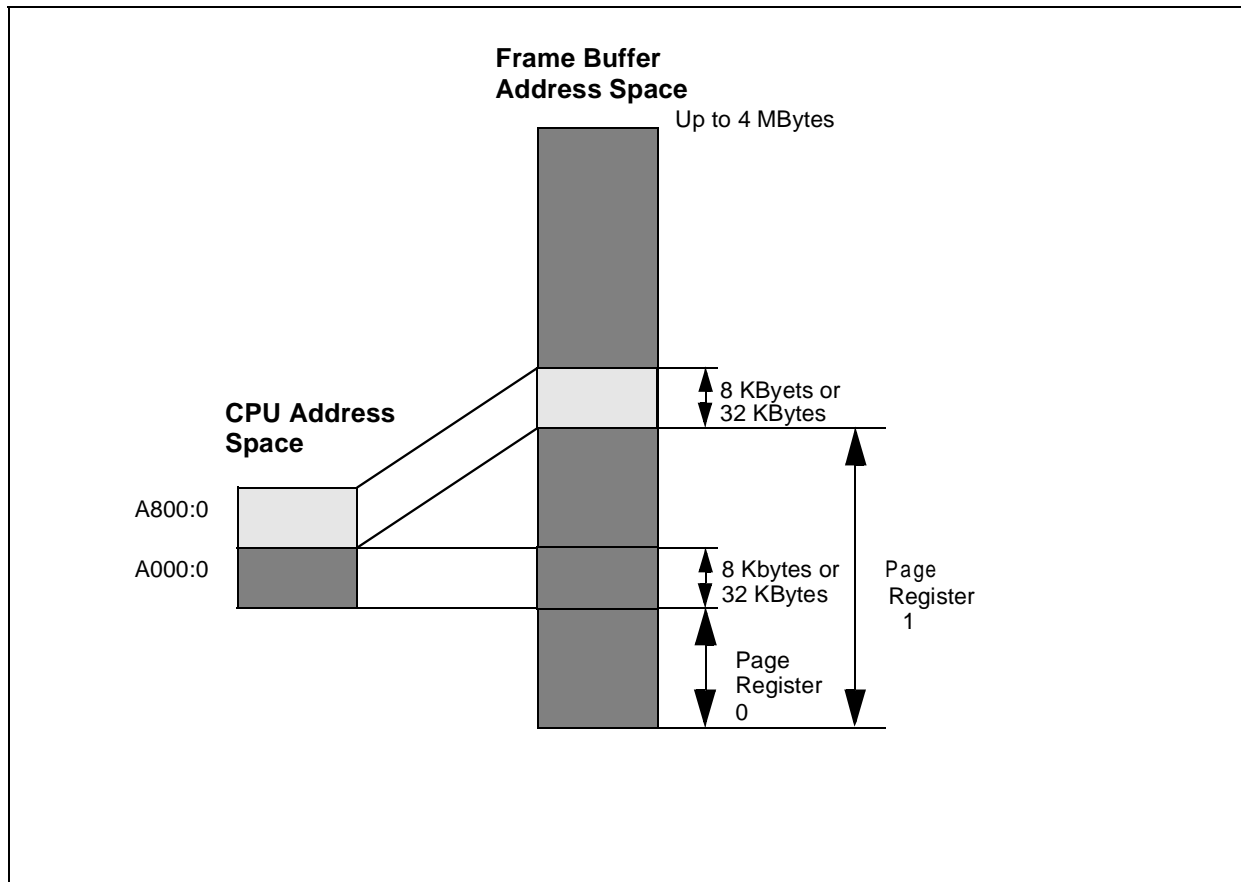


Figure 12-2. Illustration of Page Register 0 and Page Register 1

VGA CONTROLLER

12.9.7. GRAPHICS EXTENDED ENABLE REGISTER (RW)

CR1F

Access = 0x3X4h/0x3X5h

Regoffset = 01Fh

7	6	5	4	3	2	1	0
E	Rsv						
Default value after reset =00h							

Bit Number	Mnemonic	Description
Bit 7	E	Exten. Writing a '1' in this bit enables the GE extended functionality and also direct access to the frame buffer as defined by GBASE (CR20). Writing a '0' disables it. After reset, this bit is set to '0'.
Bits 6-0	Rsv	Reserved , read as '0'.

Programming notes:

The contents of this register are not altered by drawing operations.

12.9.8. GRAPHICS EXTENDED GBASE REGISTER (RW)

CR20

Access = 0x3X4h/0x3X5h

Regoffset = 020h

7	6	5	4	3	2	1	0
Rsv					G		
Default value after reset =00h							

Bit Number	Mnemonic	Description
Bits 7-3	Rsv	Reserved , these bits read as '0'.
Bits 2-0	G	Gbase . This range defines the bits 26 to 24 of the CPU address space where the GE Extended Frame Buffer and registers are located.

Programming notes:

The contents of this register are not altered by drawing operations.

VGA CONTROLLER

12.9.9. GRAPHICS EXTENDED APERTURE REGISTER (RW)

CR21

Access = 0x3X4h/0x3X5h

Regoffset = 021h

7	6	5	4	3	2	1	0
A							
Default value after reset =FFh							

Bit Number	Mnemonic	Description
Bits 7-0	A	Aperture. The lower 6 address bits are appended to the 16 least significant address bits in A0000h addresses to form a 22-bit address. This address is then used to map into the 4 MBytes Extended GE Register space. To use this feature, bits 7-6 must be set to '01'. Setting this register to FFh disables the aperture. Other values of this register can cause undefined results. The purpose of the aperture is to enable access to the extended memory mapped register in real mode.

Programming notes:

The contents of this register are not altered by drawing operations.

12.9.10. REPAINT CONTROL REGISTER 4 (RW)

CR25

Access = 0x3X4h/0x3X5h

Regoffset = 025h

7	6	5	4	3	2	1	0
Rsv		Rsv	HB	VB	VR	VD	VT
Default value after reset =FFh							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved, read as '0's.
Bit 5	Rsv	Reserved.
Bit 4	HB	Bit 6 of the 7-bit wide Horizontal Blanking End register.
Bit 3	VB	Bit 10 of the 11-bit wide Vertical Blanking start register.
Bit 2	VR	Bit 10 of the 11-bit wide Vertical Retrace start register.
Bit 1	VD	Bit 10 of the 11-bit wide Vertical Display end register.
Bit 0	VT	Bit 10 of the 11-bit wide Vertical Total register.

VGA CONTROLLER

12.9.11. REPAINT CONTROL REGISTER 5 (RW)

CR27

Access = 0x3X4h/0x3X5h

Regoffset = 027h

7	6	5	4	3	2	1	0
FIFO HWM					Rsv		
Default value after reset =D0h							

Bit Number	Mnemonic	Description
Bits 7-3	FIFO HWM	FIFO High Water Mark. When the FIFO occupancy rises above this value, the CRTC will stop filling the FIFO. This field should only ever be set by the BIOS during mode switches. Do not set this register to a value greater than the default value D0h - nothing will work.
Bits 2-0	Rsv	Reserved, read as '0'.

12.9.12. PALETTE CONTROL REGISTER (RW)

CR28

Access = 0x3X4h/0x3X5h

Regoffset = 028h

7	6	5	4	3	2	1	0
DAC PD	DAC S	SPD	Rsv	LUT B	P F		
Default value after reset =08h							

Bit Number	Mnemonic	Description
Bit 7	DAC PD	DAC Power Down. Setting this bit to one turns off the digital to analog converters. This is useful for when a second graphics card is installed in the system and power needs to be saved by turning the motherboard graphics off.
Bit 6	DAC S	DAC Setup. This bit specifies the blanking pedestal. Zero indicates a blanking pedestal of 0 IRE, one indicates 7.5 IRE.
Bit 5	SPD	Sense Power Down. Setting this bit to one forces the DDC monitor sense circuits to power down.
Bit 4	Rsv	Reserved. Must be written to '1'.
Bit 3	LUT B	LUT Bypass. Setting this bit to one bypasses the RAMDAC look up table (LUT) and allows pixels to drive the DACs directly. When this bit is set to zero the look up table is used to compute final pixel colours. This provides palette functionality for 8 bit and other low colour modes and gamma correction (non-linearity compensation) for the 24 and 32 bit true colour modes.
Bits 2-0	P F	Pixel Format. These 3-bits specify the pixel colour depth and are encoded as given in Table 12-19 .

Table 12-19. Pixel Format

Bit 2	Bit 1	Bit 0	Pixel Format
0	0	0	VGA standard 8 bit
0	0	1	8 bit colour (non-VGA)
0	1	0	15-bit (555) direct colour
0	1	1	16-bit (565) direct colour
1	0	0	24-bit (888) direct colour
1	0	1	32-bit (8888) direct colour
	1	X	Reserved

Programming notes:

For 15-bit and 16-bit pixels, the 5 or 6 bits per colour are shifted left by 3 or 2 bits and then presented to the 8-bit DACs or LUT address (depending on bit 3 above). The least significant bits are set to zero.

VGA CONTROLLER

The following resolutions are supported at 75 Hz refresh rate for each of the above colour depths when a 64 bit bank of SDRAM is used for the frame buffer.

Pixel Format	Maximum Resolution
VGA (other than mode 13)	1024 x 768
VGA (mode 13)	640 x 480
8 bit (non-VGA)	1024 x 768
15 bit	1024 x 768
16 bit	1024 x 768
24 bit	800 x 600
32 bit	640 x 480

Interlaced monitors and timings are supported.

12.9.13. CURSOR HEIGHT REGISTER

For the description of this register, see section [13.11.1. on page 290](#).

Must be written to '0' when not using a Hardware cursor.

12.9.14. CURSOR COLOUR 0 REGISTER A

For the description of this register, see section [13.11.2. on page 291](#).

Must be written to '0' when not using a Hardware cursor.

12.9.15. CURSOR COLOUR 0 REGISTER B

For the description of this register, see section [13.11.3. on page 292](#).

Must be written to '0' when not using a Hardware cursor.

12.9.16. CURSOR COLOUR 0 REGISTER C

For the description of this register, see section [13.11.4. on page 293](#).

Must be written to '0' when not using a Hardware cursor.

12.9.17. CURSOR COLOUR 1 REGISTER A

For the description of this register, see section [13.11.5. on page 294](#).

Must be written to '0' when not using a Hardware cursor.

12.9.18. CURSOR COLOUR 1 REGISTER B

For the description of this register, see section [13.11.6. on page 295](#).

Must be written to '0' when not using a Hardware cursor.

12.9.19. CURSOR COLOUR 1 REGISTER C

For the description of this register, see section [13.11.7. on page 296](#).

Must be written to '0' when not using a Hardware cursor.

12.9.20. GRAPHICS CURSOR ADDRESS REGISTER 0

For the description of this register, see section [13.11.8. on page 297](#).

Must be written to '0' when not using a Hardware cursor.

12.9.21. GRAPHICS CURSOR ADDRESS REGISTER 1

For the description of this register, see section [13.11.9. on page 298](#).

Must be written to '0' when not using a Hardware cursor.

12.9.22. GRAPHICS CURSOR ADDRESS REGISTER 2

For the description of this register, see section [13.11.10. on page 299](#).

Must be written to '0' when not using a Hardware cursor.

VGA CONTROLLER

12.9.23. URGENT START REGISTER (RW)

CR33

Access = 0x3X4h/0x3X5h

Regoffset = 033h

7	6	5	4	3	2	1	0
USP							
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-0	USP	Urgent Start Position. These bits represent the horizontal character count value at which urgency information will start to be generated for CRTC fetch requests. Prior to this position and after display enable negates, any CRTC fetches performed will be generated at low priority - i.e.. any CPU or blit operation will take precedence over CRTC regardless of CRTC FIFO occupancy. Once the horizontal character counter reaches this value, if CRTC FIFO occupancy is still below its low water mark then urgent fetches will be performed. Thereafter (and until the next display enable drops), as the CRTC FIFO drains, CRTC fetches will be marked urgent whenever the FIFO occupancy drops below its low water mark.

Programming notes:

A value of 0xFFh means "always urgent" and should be used if the VGA screen is showing "Glitches". By setting this value, the CPU and GE bandwidth will be reduced.

12.9.24. DISPLAYED FRAME Y OFFSET 0 REGISTER (RW)

CR34

Access = 0x3X4h/0x3X5h

Regoffset = 034h

7	6	5	4	3	2	1	0
F Y O							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	F Y O	Frame Y Offset 0 Bits 7-0. These bits represent bits 7-0 of a (2's complement) 16 bit scan line offset of the displayed frame relative to the Graphics Engine destination base.

VGA CONTROLLER

12.9.25. DISPLAYED FRAME Y OFFSET 1 REGISTER (RW)

CR35

Access = 0x3X4h/0x3X5h

Regoffset = 035h

7	6	5	4	3	2	1	0
F Y O							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	F Y O	Frame Y Offset 1 Bits 7-0. These bits represent bits 15-8 of the displayed frame scan line offset relative to the Graphics Engine destination base.

12.9.26. INTERLACE HALF FIELD START REGISTER (RW)

CR39

Access = 0x3X4h/0x3X5h

Regoffset = 039h

7	6	5	4	3	2	1	0
I H C							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	I H C	<p>Interlace Horizontal Count. This register defines the horizontal character count at which vertical timing is clocked during odd frames. When using interlaced operation, this register should be programmed to approximately half of the horizontal total value (CR0).</p> <p>There is no explicit interlace enable bit. Rather, when this register is programmed to FFh, interlace is disabled. The value of this register is defined to be FFh after reset (interlace disabled).</p>

VGA CONTROLLER

12.9.27. IMPLEMENTATION NUMBER REGISTER (R)

CR3A

Access = 0x3X4h/0x3X5h

Regoffset = 03Ah

7	6	5	4	3	2	1	0
I N							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	I N	Implementation Number. Indicates the hardware implementation number for the graphics drawing and display subsystem. Table 12-20 describes the interpretation of each value.

Table 12-20. Implementation Number

Value	Implementation
01h	STPC Implementation

12.9.28. GRAPHICS VERSION REGISTER (R)

CR3B

Access = 0x3X4h/0x3X5h

Regoffset = 03Bh

7	6	5	4	3	2	1	0
GVN							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	GVN	Graphics Version Number. Indicates the hardware version number for the graphics drawing and display subsystem. Table 12-21 describes the interpretation of each value.

Table 12-21. Graphics Version Number

Value	Implementation
01h	STPC Implementation

VGA CONTROLLER

12.9.29. MISCELLANEOUS TEST REGISTER

CR3E

Access = 0x3X4h/0x3X5h

Regoffset = 03Eh

7	6	5	4	3	2	1	0
Rsv							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	Rsv	Reserved. Must be set to '0'.

12.9.30. DDC CONTROL REGISTER (RW)

CR3F

Access = 0x3X4h/0x3X5h

Regoffset = 03Fh

7	6	5	4	3	2	1	0
DDC WD		DDC RD		NTSCQ (STPCC5 Version only)	COL_SEL (STPCC5 Version only)		Rsv
Default value after reset = FFh							

Bit Number	Mnemonic	Description
Bits 7-6	DDC WD	DDC Write Data. These two bits drive the DDC[1:0] <i>Direct Data Channel Serial Link</i> pins. These bidirectional pins are connected to CRTC register 3Fh to implement DDC capabilities. They conform to I ² C electrical specifications and have open-collector output drivers which are internally connected to V _{DD} through pull-up resistors. Writes to these bits affect the DDC[1:0] pins. Thus, programming either of these bits to a one disables the output driver and allows the pin to act as an input whose status can be read via bits 5-4 of this register. They can instead be used for accessing I ² C devices on board. DDC1 and DDC0 correspond to SCL and SDA respectively. Note that reads from these bits return the value of data last written to this register. This may not be the same as the data actually on the bus if another master is driving it. Bits 5-4 of this register accurately reflect the data on the bus no matter what is driving it.
Bits 5-4	DDC RD	DDC Read Data. These read-only bits return the read status of the DDC[1:0] pins.
Bits 3-1(STPCC4 Version only)	Rsv	Reserved. These bits are both readable and writable and must be programmed to ones to ensure future compatibility.
Bit 3 (STPCC5 Version)	NTSCQ	NTSC Quality: Used in conjunction with TV Horizontal Active Video Start B Register CR42 Bit 5 (Section 12.9.33. on page 229). See Table 12-22.
Bits 2-1(STPCC5 Version only)	COL_SEL	Colour Select: Bit 2 Bit 1 Colour Select Output 0 0 0 0 1 0 1 0 1 1 1 Colour Select from video (default)
Bit 0	Rsv	Reserved. This bit must be programmed to '1' for correct operation.

Table 12-22. NTSC Quality (STTPC5 Version only)

Mode	CR3F Bit 3	CR42 Bit 5	Description	
Normal (default)	1	0	Internal CRTC	Buffers open
NTSC Enabled	0	1	External CRTC	Buffers open
External Sync	0	0	External CRTC	Buffers closed
DO NOT USE	1	1	Internal CRTC	Buffers closed

VGA CONTROLLER

12.9.31. TV INTERFACE CONTROL REGISTER (RW)

CR40

Access = 0x3X4h/0x3X5h

Regoffset = 040h

7	6	5	4	3	2	1	0
TV IE	CCIR 656 E	VE	BTOE	VTV_HSYNC	FFA		
Default value after reset = FFh							

Bit Number	Mnemonic	Description
Bit 7	TV IE	TV Interface Enable. This bit enables the TV interface when set high.
Bit 6	CCIR 656 E	CCIR-656 Enable. When set to one, this bit enables the generation of CCIR-656 compatible timing codes onto the output pixel stream.
Bit 5	VE	Video Enable (active low). This bit multiplexes the TV output port between the graphics pipeline (bit 5 = '1') and the video input port (bit 5 = '0').
Bit 4: STPCC4 Version Only:	BTOE	Bottom/Top Output Enable. This bit controls the direction of the VTV_BT signal. When set to a one, VTV_BT is an output and is driven by the TV interface's timing generator. Note that External Timing Generator 1 , bit 29 also controls the direction of this signal. The truth table is as follows (see Table 12-23).
Bit 4: STPCC5 Version Only:		VSYNC(BT) see Section 12.9.33. for detailed application
Bit 3: STPCC4 Version Only:	VTV_HSYNC	VTV_HSYNC Output Enable. This bit controls the direction of the VTV_HSYNC signal. When set to a one, VTV_HSYNC is an output and is driven by the TV interface's timing generator. Note that Video Input Port register 2B, bit 28 also controls the direction of this signal. The truth table is as follows (see Table 12-24)
Bit 3: STPCC5 Version Only:		HSYNC see Section 12.9.33. for detailed application
Bits 2-0	FFA	Flicker Filter Algorithm. These bits control the operation of the anti-flicker filter according to Table 12-25

Table 12-23. VTV_BT Signal Direction

CR40 Bit [4]	vtg_ext1 Bit [29]	VTV_BT direction
0	0	input
0	1	output from VIP t/g
1	X	output from TVO t/g

Table 12-24. VTV_HSYNC Signal Direction

CR40 Bit [3]	vtg_ext1 Bit [28]	VTV_HSYNC direction
0	0	input
0	1	output from VIP t/g
1	X	output from TVO t/g

Table 12-25. Anti-Flicker Filter Operation

Bit 2	Bit 1	Bit 0	Function
X	0	0	Filter disabled
0	0	1	0:1:1 2 tap filter
0	1	0	1:2:1 3 tap filter
0	1	1	1:3:1 3 tap filter
1	0	1	0:1:1 2 tap filter -Y only
1	1	0	1:2:1 3 tap filter - Y only
1	1	1	1:3:1 3 tap filter - Y only

VGA CONTROLLER

12.9.32. TV HORIZONTAL ACTIVE VIDEO START A REGISTER (RW)

CR41

Access = 0x3X4h/0x3X5h

Regoffset = 041h

7	6	5	4	3	2	1	0
TV							
Default value after reset =							

Bit Number	Mnemonic	Description
Bits 7-0	TV	These are bits [7:0] of the eleven bit wide horizontal active video start field. This field controls the positioning of the left hand side of the active TV display - to a one pixel granularity.

12.9.33. TV HORIZONTAL ACTIVE VIDEO START B REGISTER (RW)

CR42

Access = 0x3X4h/0x3X5h

Regoffset = 042h

7	6	5	4	3	2	1	0
Rsv	Rsv		See Below	TV	WH		
Default value after reset =							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved. For test and/or debug purposes, this bit may be used to reverse the order of chrominance and luminance bytes in the output stream. Normal operation requires this bit to be written as a zero.
Bits 6-5	Rsv	Reserved. These read/write bits should be written as zeroes to ensure future compatibility.
Bit 4: STPCC4 Version Only:	Rsv	Reserved. These read/write bits should be written as zeroes to ensure future compatibility.
Bit 4: STPCC5 Version Only:	TVHAB	TV Horizontal Active Video Start B. It is possible to unlink the either the HSYNC and the VSYNC signals between the Video Input Port and the Digital Encoder. The supported modes are shown in Table below. In order to have the complete function, Register CR40 in Section 12.9.31. and CR28 in Section 12.9.12.
Bit 3	TV	TV output mode. This bit defines the output format on the four analog DAC outputs of the TV encoder. This bit defaults to zero on reset (see Table 12-27).
Bits 2-0	WH	These represent bits 10:8 of the eleven bit Wide Horizontal active video start field. See 12.9.32. on page 228.

Table 12-26. TV Horizontal Active Video Start B Modes

Mode	TVHA bit 4	TVIC bit 4/3	VIPETG bit 29/28	Operation
Input 601 mode	0	0	0	Vsync (BT) and Hsync come from the external pads (CCIR 601) and go to VIP and DENC (pass through)
Input 656 mode	0	0	1	Vsync (BT) and Hsync come from the VIP (CCIR 656) and go to the DENC (pass through). Pads are outputs (VIP)
TV output	0	1	X	Vsync (BT) and Hsync come from the TV output. VIP sync lines are busy, thus the VIP can not be configured in the same mode as the TV output (CCIR 656/CCIR 601 or reversed). Pads are outputs (TVO)
Pipeline 601	1	0	0	Same as Input 601 mode but the DENC sync come from the TV output (CCIR 656 possible). Pads are inputs.
Pipeline 656	1	0	1	Same as Input 656 mode but the DENC sync come from the TV output (CCIR 601 possible). Pads are outputs (VIP)
TV independent output	1	1	X	Vsync (BT) and Hsync from the TV output to the DENC are independent from the VIP but are output on the pads and input to the VIP (crossed mode CCIR 601/656 not possible).

Table 12-27. TV Output Mode

Bit 3	RED_TV	GREEN_TV	BLUE_TV	CVBS
0	red	green	blue	composite
1	chrominance	luminance	composite	composite

12.9.34. TV HORIZONTAL SYNC END A REGISTER (RW)

CR43

Access = 0x3X4h/0x3X5h

Regoffset = 043h

7	6	5	4	3	2	1	0
WH							
Default value after reset =							

Bit Number	Mnemonic	Description
Bits 7-0	WH	These are bits [7:0] of the eleven bit Wide Horizontal sync end field. This field represents the width, in pixels, of the (interlaced) HSYNC signal produced by the TV interface. Bit 3 of CR40 controls whether this interlaced hsync is actually output.

VGA CONTROLLER

12.9.35. TV HORIZONTAL SYNC END B REGISTER (RW)

CR44

Access = 0x3X4h/0x3X5h

Regoffset = 044h

7	6	5	4	3	2	1	0
Rsv	Rsv	Rsv			WH		
Default value after reset =							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved. This bit should be programmed to be the same as CR10 bit 0. It is separately programmable purely for test and / or debug purposes.
Bit 6	Rsv	Reserved. This bit, when set to one, allows the luminance output of the colourspace converter (progressive scan) to be directly output onto the TV_YUV output bus. This is for test/debug use only and this bit should normally only ever be programmed to zero.
Bits 5-3	Rsv	Reserved. These read/write bits should be written as zeroes to ensure future compatibility.
Bits 2-0	WH	These represent bits 10:8 of the eleven bit Wide Horizontal sync end field.

12.10. ADDITIONAL MODES

12.10.1. FAST 132 CHARACTER WIDE TEXT MODE.

To meet the high bandwidth requirements of 132 column text mode, VGA Controller supports a special high speed text mode. For column widths of 96 characters and greater, bit 7 of extended register CR1C - the Repaint Control Register #3 must be set to one prior to loading the font tables into frame buffer plane two. Fonts may then be loaded in the standard VGA manner one Byte at a time at the end of which bit 7 of CR1C should be reset to zero.

Setting bit 7 of CR1C to one performs an address warping such that standard VGA font load cycles actually store fonts into plane two the following way:

Byte 0: Character Set 0, Font (ASCII) 0, Line 0

Byte 1: Character Set 0, Font (ASCII) 1, Line 0

...

Byte 255: Character Set 0, Font 255, Line 0

Byte 256: Character Set 1, Font (ASCII) 0, Line 0

...

Byte 511: Character Set 1, Font 255, Line 0

Byte 512: Character Set 2, Font (ASCII) 0, Line 0

...

Byte 2047: Character Set 7, Font 255, Line 0

Byte 2048: Character Set 0, Font (ASCII) 0, Line 1

Applications which load their own fonts independent of the motherboard BIOS will not be supported in 132 column modes because of the above requirements.

Note that the above organization of font data will ensure that 132 column mode bandwidth requirements are low enough to be satisfied by 64 bit wide SDRAM Frame Buffers only. If the frame buffer is 32 bits wide, then the primary and secondary character map selects (SR3) should only ever be programmed such that both of the primary and secondary fonts are in the range 0-3 or both are in the range 4-7. Failure to observe this requirement will result in a garbaged screen.

12.11. INTERLACED MONITOR SUPPORT

Section 4.7.6.26a describes the "interlace half field start" register field. Setting this field to a value other than FFh (the power on reset default) enables interlaced CRT timing generation.

In interlaced timing mode, the horizontal and vertical timing parameters (CR0-CR7, CR10-CR12, CR15, CR16) should be programmed to values equal to what they would otherwise take in non-interlaced modes with the following modifications:

- Horizontal period must be an even number of character clocks. This results in the requirement that CR0[0] must equal '1'.
- Interlace half field start (CR39) must be set equal to $CR4 - (CR0 + 5)/2$.
- Vertical period must be an odd number of scan lines. That is, CR6[0] must be set to 1.
- Vertical overscan period should be an even number of scan lines. That is the vertical blank start field must be odd (CR15[0] = '1') and vertical blank end field must be even (CR16[0] = '0'). If this is not

VGA CONTROLLER

observed the top and bottom lines of the border will be only half a scan line wide on alternate fields. If no border will be displayed then there is no restriction on vertical blank start and end.

All other registers should be programmed as they would for the same resolution and colour depth in non-interlaced mode.

12.12. RAMDAC REGISTERS**12.12.1. PALETTE PIXEL MASK REGISTER (RW)**

This eight-bit mask register is ANDed with the pseudo-colour pixel before doing the palette look-up. This provides an alternate way of altering the displayed colours without changing the display memory or colour palette.

<i>Pixel_Mask</i>		Access = 0x3C6h				Regoffset =	
7	6	5	4	3	2	1	0
Default value after reset = FFh							

VGA CONTROLLER

12.12.2. PALETTE READ INDEX REGISTER (W)

This register contains the index value for the read access to the 256 entries of the colour palette. Each entry is 24-bits wide (8-bits each for R, G and B) and is read as sequence of three Bytes. After writing the index of the entry to be read, the actual contents of the selected palette entry are read by doing three consecutive Byte reads from the DAC Data port (3C9h) in sequence: 1) Red, 2) Green and 3) blue. This 3-Byte read sequence is aborted and a new one is started if either the Read or Write Index register is written before reading the third Byte.

After the third Byte of the sequence is read, the index register is automatically incremented to point to the next entry of the look-up table. If the index is FFh, it rolls over to 00h.

This register is a write only register. Reads from this address do not return the contents of the index register. The Palette state register contents are returned instead.

Read_Index				Access = 0x3C7h		Regoffset =	
7	6	5	4	3	2	1	0
Default value after reset =							

12.12.3. PALETTE STATE REGISTER (R)

This is a read only register and contains the two least significant bits of the last IO writes to IO address 3C6h-3C9h.

Palette_State

Access = 0x3C7h

Regoffset =

7	6	5	4	3	2	1	0
Rsv						IO	
Default value after reset =							

Bit Number	Mnemonic	Description
Bits 7-2	Rsv	Reserved. The read back of this register is undefined.
Bit 1-0	IO	These bits contain the 2 LSBs of the address of the last IO write to ports 3C7h or 3C8h. '00' indicate that the last write was to port 3C8h, '11' indicate 3C7h.

VGA CONTROLLER

12.12.4. PALETTE WRITE INDEX REGISTER (RW)

This register is similar to the Read index register and contains the index value for the write access to the 256 entries of the colour palette. Each entry is 24-bit wide and are written as a sequence of 3-Bytes. After writing the index of the entry to be modified, the data values may be written to the DAC Data port (3C9h) in the sequence: 1) Red, 2) Green, and 3) Blue. This 3-Byte write sequence is aborted and new one is started if either the Read or Write Index register is written before writing the third Byte.

After the third Byte of the sequence is written, the index register is automatically incremented to point to the next entry of the look-up table. If the index is FFh, it rolls over to 00h.

Both the Read and the Write index registers, physically map to a single index register. However only the Write Index register can be read. Reads from the Read Index register return the contents of Palette state register.

<i>Write_Index</i>				Access = 0x3C8h		Regoffset =	
7	6	5	4	3	2	1	0
Not initialised by reset							

12.12.5. PALETTE DATA REGISTER (RW)

This register is used in conjunction with the Read and the Write index register to access the look-up table. Reads from this port return the contents of the entry pointed to by the Read Index register and writes to this port modify the content of the look-up table entry pointed to by the Write Index register. Each look-up table entry is 24-bit wide and is read or written as a sequence of three Bytes. The read or write sequence is always Red, Green and Blue. The normal procedure for accessing the look-up table is to initialise one of the Index registers and follow it with an uninterruptible sequence of three reads/writes from this register.

For VGA backward compatibility, when bits 2-0 of CR28 are programmed to 000 (as they are after reset), the palette look up table is treated as if each entry was only 18 bits wide. In this case, writes to port 3C9h map data such that bits 5-0 of host data are written into bits 7-2 of the look-up table while bits 1-0 are zeroed out. Similarly, reads return bits 7-2 of look-up table data onto host bits 5-0 and zero out bits 7-6.

When bit 5 of register CR3E is set to one, reads and writes to this port access red, green and blue signature data instead of look-up table data.

To minimise the sparkle while accessing the look-up table, all three bytes are read or written in a single video clock interrupting the screen repaint for one clock only. The interrupted pixel is painted with the same colour as the previous pixel.

Palette_Data			Access = 0x3C9h			Regoffset =	
7	6	5	4	3	2	1	0
Not initialised by reset							

VGA CONTROLLER

12.13 DCLK Control registers

These registers control the Dot Clock or pixel clock which the VGA uses to display the pixels on the screen.

12.13.1. DCLK Control Register 00

This is one of the 4-pairs of Dot Clock Control registers. This pair (00 and 01) is selected when bits 3-2 of VGA Miscellaneous Output register is set to 00.

DCLK00		Access = 022h/023h				Regoffset =42h	
7	6	5	4	3	2	1	0
Rsv	4BD				8BN		
Default value after reset = 0x76h							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved.
Bits 6-3	4BD	This is the 4-bit M (divisor) value of the Dot Clock Synthesiser.
Bits 2-0	8BN	These are bits 7-5 of the 8 bit N (multiplier) of the Dot Clock synthesiser.

Programming notes:

This register defaults to 0x76h at reset. This value when combined with the default value of the other half of this pair results in a Dot Clock of 25.18 MHz assuming 14.318 MHz oscillator clock as the reference input.

$$DCLK = \frac{2 \times 14.31818 \times N}{M \times 2^P}$$

Constraints: $1 \leq M \leq 255$
 $1 \leq N \leq 255$
 $0 \leq P \leq 5$

$$1 \text{ MHz} \leq \frac{14.31818}{M} \leq 2 \text{ MHz}$$

$$200 \text{ MHz} \leq \frac{2 \times 14.31818 \times N}{M} \leq 622 \text{ MHz}$$

12.13.2. DCLK control register 01

This is one of the 4-pairs of Dot Clock Control registers. This pair (00 and 01) is selected when bits 3-2 of VGA Miscellaneous Output register is set to 00.

DCLK01

Access = 022h/023h

Regoffset =43h

7	6	5	4	3	2	1	0
3BP0	8BN					3BP1	
Default value after reset = 0x95h							

Bit Number	Mnemonic	Description
Bit 7	3BP0	This is the bit 0 of the 3-bit P (exponent) value of the Dot clock synthesiser.
Bits 6-2	8BN	These are bits 4-0 of the 8-bit N (multiplier) value of the Dot Clock Synthesiser.
Bits 1-0	3BP1	These are bits 2-1 of the 3-bit P (exponent) value of the Dot clock synthesiser.

Programming notes:

This register defaults to 0x95h at reset. This value when combined with the default value of the other half of this pair results in a Dot Clock of 25.18 MHz assuming 14.318 MHz oscillator clock as the reference input.

VGA CONTROLLER

12.13.3. DCLK control register 10

This is one of the four pairs of dot clock control registers. This pair (10 and 11) is selected when bits 3-2 of VGA Miscellaneous Output register is set to 01.

DCLK10

Access = 022h/023h

Regoffset =44h

7	6	5	4	3	2	1	0
Rsv	4BM				8BN		
Default value after reset = 0x76h							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved.
Bits 6-3	4BM	This is the 4-bit M (divisor) value of the Dot Clock Synthesiser.
Bits 2-0	8BN	These are bits 7-5 of the 8 bit N (multiplier) of the Dot Clock Synthesiser.

Programming notes:

This register defaults to 0x76h at reset. This value when combined with the default value of the other half of this pair results in a Dot Clock of 28.0 MHz assuming 14.318 MHz oscillator clock as the reference input.

12.13.4. DCLK control register 11

This is one of the four pairs of Dot Clock Control registers. This pair (10 and 11) is selected when bits 3-2 of VGA Miscellaneous Output register is set to 01.

DCLK11

Access = 022h/023h

Regoffset =45h

7	6	5	4	3	2	1	0
3BP0	8BN					3BP1	
Default value after reset = 0xEDh							

Bit Number	Mnemonic	Description
Bit 7	3BP0	This is the bit 0 of the 3-bit P (exponent) value of the Dot Clock Synthesiser.
Bits 6-2	8BN	These are bits 4-0 of the 8-bit N (multiplier) value of the Dot Clock Synthesiser.
Bits 1-0	3BP1	These are bits 2-1 of the 3-bit P (exponent) value of the Dot Clock Synthesiser.

Programming notes:

This register defaults to 0xEDh at reset. This value when combined with the default value of the other half of this pair results in a Dot Clock of 28.0 MHz assuming 14.318 MHz oscillator clock as the reference input.

VGA CONTROLLER

12.13.5. DCLK control register 20

This is one of the four pairs of Dot Clock Control registers. This pair (20 and 21) is selected when bits 3-2 of VGA Miscellaneous Output register is set to 10.

DCLK20

Access = 022h/023h

Regoffset =46h

7	6	5	4	3	2	1	0
Rsv	4BM				8BN		
Default value after reset = 0x5Bh							

Bit number	Mnemonic	Description
Bit 7	Rsv	Reserved.
Bits 6-3	4BM	This is the 4-bit M (divisor) value of the Dot Clock Synthesiser.
Bits 2-0	8BN	These are bits 7-5 of the 8 bit N (multiplier) of the Dot Clock Synthesiser.

Programming notes

This register defaults to 0x5Bh at reset. This value when combined with the default value of the other half of this pair results in a dot clock of 40 MHz assuming 14.318 MHz oscillator clock as the reference input.

12.13.6. DCLK control register 21

This is one of the four pairs of Dot Clock Control registers. This pair (20 and 21) is selected when bits 3-2 of VGA Miscellaneous Output register is set to 10.

DCLK21

Access = 022h/023h

Regoffset =47h

7	6	5	4	3	2	1	0
3BP0	8BN					3BP1	
Default value after reset = 0x6Dh							

Bit Number	Mnemonic	Description
Bit 7	3BP0	This is the bit 0 of the 3-bit P (exponent) value of the Dot Clock Synthesiser.
Bits 6-2	8BN	These are bits 4-0 of the 8-bit N (multiplier) value of the Dot Clock Synthesiser.
Bits 1-0	3BP1	These are bits 2-1 of the 3-bit P (exponent) value of the Dot Clock Synthesiser.

Programming notes:

This register defaults to 0x6Dh at reset. This value when combined with the default value of the other half of this pair results in a Dot Clock of 40 MHz assuming 14.318 MHz oscillator clock as the reference input.

VGA CONTROLLER

12.13.7. DCLK control register 30

This is one of the four pairs of dot clock control registers. This pair (30 and 31) is selected when bits 3-2 of VGA Miscellaneous Output register is set to 11.

DCLK30

Access = 022h/023h

Regoffset =48h

7	6	5	4	3	2	1	0
Rsv	4BM				8BN		
Default value after reset = 0x6Eh							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved.
Bits 6-3	4BM	This is the 4-bit M (divisor) value of the Dot Clock Synthesiser.
Bits 2-0	8BN	These are bits 7-5 of the 8 bit N (multiplier) of the Dot Clock Synthesiser.

Programming notes:

This register defaults to 0x6Eh at reset. This value when combined with the default value of the other half of this pair results in a Dot Clock of 60 MHz assuming 14.318 MHz oscillator clock as the reference input.

12.13.8. DCLK control register 31 DCKL31 Index 49

This is one of the four pairs of dot clock control registers. This pair (30 and 31) is selected when bits 3-2 of VGA Miscellaneous Output register is set to 11.

DCLK31

Access = 022h/023h

Regoffset =49h

7	6	5	4	3	2	1	0
3BP0	8BN					3BP1	
Default value after reset = 0x69h							

Bit Number	Mnemonic	Description
Bit 7	3BP0	This is the bit 0 of the 3-bit P (exponent) value of the Dot Clock Synthesiser.
Bits 6-2	8BN	These are bits 4-0 of the 8-bit N (multiplier) value of the Dot Clock Synthesiser.
Bits 1-0	3BP1	These are bits 2-1 of the 3-bit P (exponent) value of the Dot Clock Synthesiser.

Programming notes:

This register defaults to 0x69h at reset. This value when combined with the default value of the other half of this pair results in a Dot Clock of 60 MHz assuming 14.318 MHz oscillator clock as the reference input.

13. GRAPHICS ENGINE

13.1. INTRODUCTION

The Graphics Engine (GE) performs limited graphics drawing operations. The results of these operations change the content of the on-screen or off-screen frame buffer areas of DRAM memory.

Pixel depths of 8-bit, 16-bit, 24-bit and 32-bit are fully supported by the GE.

13.2. MEMORY ADDRESS SPACE

The extended (non-VGA) graphics and video functions of the Graphics Engine occupy 16 MBytes of memory address space. This space can be located anywhere in the memory on any 16 MByte boundary between 128 MBytes and 256 MBytes. The 16 MByte region is divided into four parts as shown in [Figure 13-1](#).

[Figure 13-1](#) shows the GBASE as Extended CRTC Register 20 (CR20) and provides bits 26 through 24 of the starting address, where the CPU sees the extended graphics and video functionality.

This 16-MByte space can be linearly (one to one) mapped in the CPU address space or can be accessed via a 64K aperture located at A0000h-AFFFFh. The aperture access method (described in more detail in the VGA Controller Section of the Programming Manual, Graphics Extended Aperture Register, CR21) facilitates the access to extended functionality in real mode.

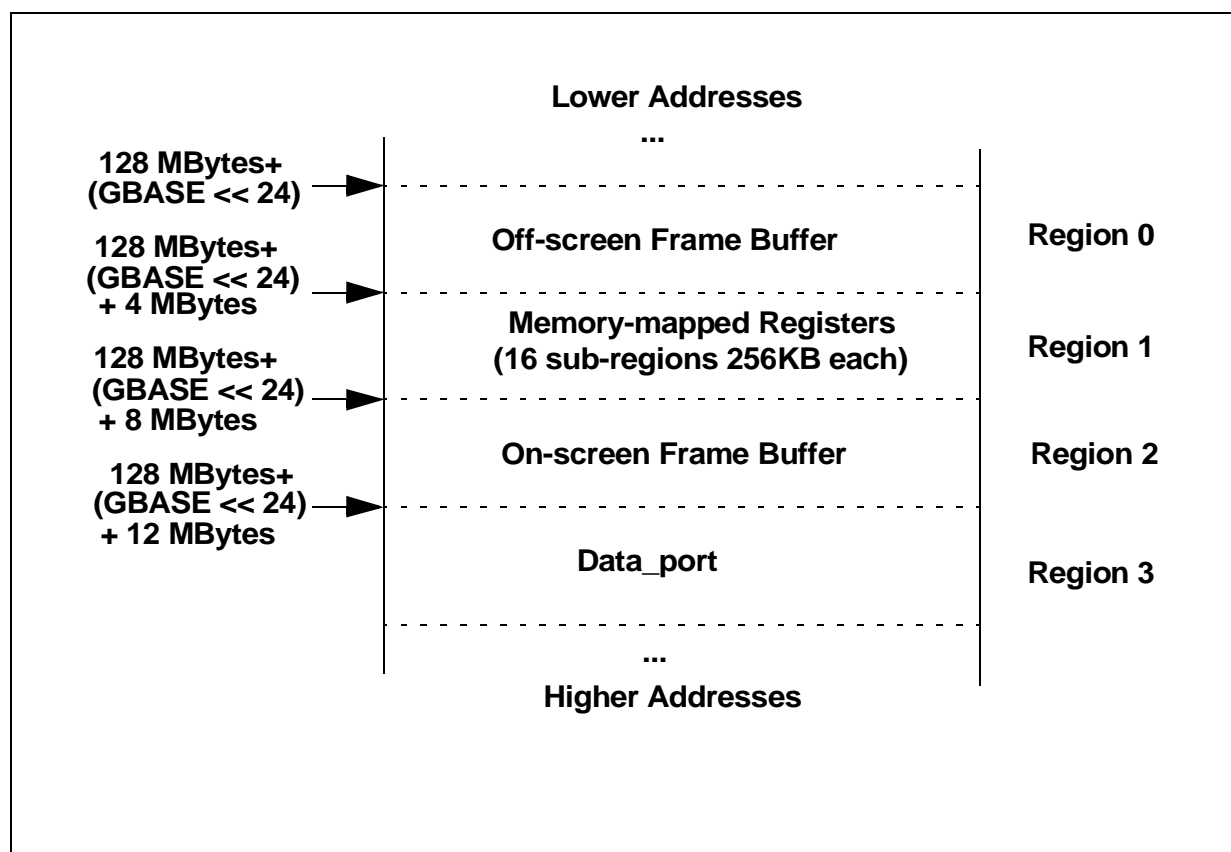


Figure 13-1. GE memory Map

GRAPHICS ENGINE

Two 4-MByte regions are dedicated to the frame buffer, which reads from either 128 MBytes + (GBASE<<24) or 128 MBytes + (GBASE<<24) + 8 MBytes, handled identically in either case.

However, writes to any area of the Frame Buffer that might be displayed should be done to the region 128 MBytes + (GBASE<<24) + 8 MBytes. Writes to areas of the Frame Buffer that are not displayed should be done to 128MBytes + (GBASE<<24). The Frame Buffer address used by the host also informs the GE whether the access is being made to an on-screen or off-screen drawing area. It is important that the software never draws using an off-screen area address to a portion of the Frame Buffer that is currently being displayed. This is necessary to maintain compatibility with future versions of the GE.

The Frame Buffer addresses loaded into GE registers are from 0 to 4 MBytes. The source, pattern or destination of a GE operation can be located anywhere in Frame Buffer DRAM. However, the DRAM physical address must be known; the entire operand must be contiguous in physical memory (the GE does not include scatter/gather), and the operands must not move from the specified memory location until the drawing operation is completed.

All registers needed for the extended graphics and video functionality are mapped in a 4-MByte region of its own. This region is further divided in 16 X 256 KByte sub-regions illustrated in [Table 13-1](#).

Table 13-1. Graphic Memory Sub-divisions

Sub-region	Region function
0	2-D Graphics Engine registers
1	Reserved
2	Video overlay registers
3-7	Reserved for future functionality
8	Video Input Port Registers
9-15	Reserved for future functionality

Writes done to any double word between (128 MBytes + (GBASE << 24) + 12 MBytes) to (128 MBytes + (GBASE << 24) + 16 MBytes) will be the same as a write to the Data_port register of the 2-D graphics engine. This region of 1 million aliases of the Data_port is provided to allow the use of string move instructions for Host-to-screen BitBlts.

All registers can be read with accesses of any width. The CPU can read any register via Byte (8-bit), word (16-bit), or double-word (32-bit) accesses. Writes must be done using double-word (32-bit) transfers.

Note that the contents of all GE registers are not defined after reset.

Software must initialise all registers upon power-up before attempting any drawing operation.

13.3. DUMB FRAME BUFFER ACCESS

The CPU can access the frame buffer memory as ordinary memory. It can read from or write to the frame buffer using any memory access instruction, and any data width. Thus, the CPU can access the frame buffer as if it were an unaccelerated display subsystem. This access by the CPU is permitted regardless of the GE busy status. Therefore, software must be careful to avoid race conditions or clashes if writing to the frame buffer when the GE is busy.

13.4. ADDRESSING

The GE frame buffer and extended registers may be accessed by the CPU via two methods: extended addresses, or A0000h-AFFFFh addresses. The former method allows direct access to the 16 MByte GE address range via 32-bit addresses. The A0000h-AFFFFh addressing method maps a 64K window of the 16 MByte GE address space into the address range A0000h-AFFFFh. For additional details on the A0000h-AFFFFh addressing, see the VGA Controller Section in the Programming Manual, Graphics Extended Aperture Register, CR21.

The Frame Buffer address used by the host also informs the GE whether the access is being made to an on-screen or off-screen drawing area. It is important that the software never draws using an off-screen area address to a portion of the Frame Buffer that is currently being displayed.

The addresses that are loaded into GE registers are the physical DRAM addresses after the OS address translation and GE host address remapping has been done. The Frame Buffer addresses loaded into GE registers are from 0 to 4 MBytes. The source, pattern or destination of a GE operation can be located anywhere in the Frame Buffer space.

13.5. VGA OPERAND SOURCES

The GE operates on data which can originate in one of three possible areas:

- 1) The frame buffer memory (i.e. a location in the DRAM memory that is dedicated to the graphics subsystem, and which may or may not be currently displayed by the CRT controller).
- 2) The host-supplied data.
- 3) The on-chip colour registers.

13.5.1. OPERAND SELECTION

Some operands are colour pixels and others are monochrome bitmaps. In general, the data written to the Destination address is the result of a Raster Operation (ROP) performed on three pixel-depth colour inputs:

- 1) The Source, which can originate from frame buffer memory (for Screen-to-screen BitBlts), from the Host (for Host-to-screen BitBlts), or from the Foreground and Background colour registers.
- 2) The pattern, which must originate from the frame buffer.
- 3) The destination, which must originate from the frame buffer.

When one or more of these operands are the inputs to an 8-bit Windows' ROP, the result is written to the destination.

If the ROP does not use a source operand, then the "Source" field of the ROP register must be set to `CONSTANT_FILL` (see ROP register [Section 13.9.11.](#)) to prevent wasted performance due to needless operand fetching.

If the ROP requires destination data reads, then the "Dst" field of the ROP register must be set to '1'. If destination reads are not required, then this field should be set to '0'.

If the ROP requires pattern data or uses colour transparent mode, then the "Pat" field of the ROP register must be set to '1'. If no pattern or colour transparency is being used in the operation, then this field should be set to '0'.

GRAPHICS ENGINE

13.5.2. TRANSPARENT MODE

Transparent mode drawing leaves some of the destination pixels untouched. The GE supports four types of transparent mode drawing:

- 1) Bitmap transparency, where bits that are '1' are expanded to the Foreground colour register value and drawn, but bits that are expanded to '0' are not drawn.
- 2) Pattern transparency, where any Pattern Bytes that are '0' suppress writing to the corresponding destination pixel Bytes.
- 3) Source transparency, where any Source pixel which either matches the value or does not match the value of the source transparency register is not drawn.
- 4) Destination transparency, where any Destination pixel that either matches the value or does not match the value of the source transparency register is not drawn.

These modes are controlled by fields in the ROP register.

13.6. VGA OPERAND FRAME BUFFER ADDRESSES

The GE fetches needed data from the frame buffer area. The software identifies these areas with an operand base address, unsigned X and Y Indices from this base address, and a pitch for that region. The pitch is the Byte distance between two pixels which are in the same X position of adjacent scan lines.

The frame buffer is addressed using DRAM linear addresses. These are the addresses that the DRAMs are presented with. The frame buffer starts at DRAM linear address 0 and continues until the top of the frame buffer. The system physical addresses are mapped to above the frame buffer. To accommodate a more natural view of the frame buffer, the GE implements X-Y addressing. An operand base address, pitch, X and Y components are combined in the GE, to form the associated DRAM linear address. The base component of an operand is the DRAM linear address at the start of that operand. Addresses can range from 0 to the maximum size of the frame buffer, depending on where the operand is located in the frame buffer.

A pixel X coordinate is usually expressed as an unsigned Byte quantity, the number of Bytes from the left edge of a scan line.

If the X_dir field of the Pixel_depth register is '0', advancing from left-to-right, then X points to the least-significant Byte of the starting pixel.

If the X_dir field of the Pixel_depth register is '1', advancing from right-to-left, then X points to the most-significant Byte of the starting pixel.

Mathematically, consider a BitBlt region that starts at (x0, y0), where "x0" is in pixels. This region is W+1 Bytes wide, is H+1 scan lines high and has BPP (Bytes-per-pixel).

Then the starting address that must be programmed into the GE is dependent on the X_dir and Y_dir fields of the Pixel_depth register. This is illustrated in [Table 13-2](#).

Table 13-2. Detail GE Starting Address Register

X_dir	Y_dir	Starting Address
0	0	(x0 * BPP, y0)
0	1	(x0 * BPP, y0 + H)
1	0	(x0 * BPP + W, Y0)
1	1	(x0 * BPP + W, Y0 + H)

Note that movement in the negative X direction (i.e. X_dir set to '1') is only defined for Screen-to-screen colour BitBlts.

When bitmap expansion is enabled, the X field of the Src_XY register is a bit address and not a Byte address. In other words, the least significant three bits of Src_XY.X refer to the bit within a Byte of bitmap data.

Internally, the GE performs calculations using the X and Y coordinates. When a DRAM linear address is needed, for example to write a destination pixel, the address is computed using:

$$\text{linear_address} = \text{operand_base} + (Y * \text{pitch}) + X * \text{BPP}$$

The multiplication by pitch is done using hardwired shifts and adds. The pitch is specified as a group of four shift codes. For each non-zero shift code, the Y address is shifted by a corresponding number of bits and then added to the total. The resulting sum is then added to X and the base address to obtain the DRAM linear address. The shift values supported are shown in [Table 13-3](#).

Table 13-3. Shift Values Supported

Value	Shift0	Shift1	Shift2	Shift3
000	0	0	0	0
001	0	0	32 * Y	1024 * Y
010	0	64 * Y	64 * Y	2048 * Y
011	128 * Y	128 * Y	128 * Y	4096 * Y
100	256 * Y	256 * Y	256 * Y	n/a
101	512 * Y	512 * Y	512 * Y	n/a
110	1024 * Y	1024 * Y	0	n/a
111	2048 * Y	0	0	n/a

The operand base addresses must be aligned to 32 Bytes (that is, the five least significant bits of the address must be zeros).

The supported pitches (in Bytes) are:

0, 32, 64, 96, 128, 160, 192, 224, 256, 288, 320, 352, 384, 416, 448, 512, 544, 576, 608, 640, 672, 704, 768, 800, 832, 896, 1024, 1056, 1088, 1120, 1152, 1184, 1216, 1248, 1280, 1312, 1344, 1376, 1408, 1440, 1472, 1536, 1568, 1600, 1632, 1664, 1696, 1728, 1792, 1824, 1856, 1920, 2048, 2080, 2112, 2144, 2176, 2208, 2240, 2272, 2304, 2336, 2368, 2400, 2432, 2464, 2496, 2560, 2592, 2624, 2656, 2688, 2720, 2752, 2816, 2848, 2880, 2944, 3072, 3104, 3136, 3168, 3200, 3232, 3264, 3328, 3360, 3392, 3456, 3584, 3616, 3648, 3712, 3840, 4096, 4128, 4160, 4192, 4224, 4256, 4288, 4320, 4352, 4384, 4416, 4448, 4480, 4512, 4544, 4608, 4640, 4672, 4704, 4736, 4768, 4800, 4864, 4896, 4928, 4992, 5120, 5152, 5184, 5216, 5248, 5280, 5312, 5376, 5408, 5440, 5504, 5632, 5664, 5696, 5760, 5888, 6144, 6176, 6208, 6240, 6272, 6304, 6336, 6400, 6432, 6464, 6528, 6656, 6688, 6720, 6784, 6912, 7168, 7200, 7232, 7296, 7424, 7680.

13.6.1. COMMAND INITIATION

The destination coordinate register, Dst_XY, appears multiple times in the address space. Reading from any of these appearances, or aliases, is equivalent. Writing to most of these aliases also has the effect of initiating a drawing command. Which command is begun depends upon the address written to. There is also an address that just provides write access to the Destination register, with no other side-effects.

The operations encoded in the Dst_XY register are shown in [Table 13-5](#), where “GBASE” is the contents of the Extended CRTC Register 20 (CR20). Bits 23 through 16 are ‘01000001’ to identify this as a Dst_XY register access. This is shown in [Table 13-4](#).

Table 13-4. CMD Operations

CMD	Operation
00	Simple BitBlt, all registers must be set up before this command is issued (the Count field is ignored)
01	Width-specified BitBlt, the Count field of the address is used as the width for the operation, all other relevant registers (height, ROP, etc.) must be set up before this command is issued
10	Height-specified BitBlt, the Count field of the address is used as the height for the operation, all other relevant registers (width, ROP, etc.) must be set up before this command is issued
11	Write to Dst_XY without starting a BitBlt operation, (used for diagnostic applications)

When the CPU writes to the Dst_XY register using one of these operation aliases, the register write is completed and then the associated operation is begun. Thus, to perform an operation, the CPU writes to all but the Destination register. Then the last write is done to the Dst_XY register using one of the above aliases.

The ROP register also has fields that control the Source data (Screen, Host or Foreground colour register), enables/disables bitmap expansion, determines if the drawing is done in one of the transparent modes.

Screen-to-screen BitBlts are done as a BitBlt with the Source set as the Screen and bitmap expansion disabled.

Host-to-screen BitBlts are done as a BitBlt with the Source set as Host and the bitmap expansion disabled.

Rectangular fills are done as a BitBlt with the Source set to the Foreground colour register and the bitmap expansion disabled.

Text drawing using bit-packed font data provided by the Host is done as BitBlt with the Source set as Host and the bitmap expansion enabled. A transparent mode may also be specified.

Lines are not generally supported by the GE, but horizontal and vertical line segments can be quickly implemented as Width-specified BitBlts with the Height register set to 0 (to indicate a single pixel high BitBlt), or as Height-specified BitBlts with the Width register set to one less than the pixel depth.

Table 13-5. Encoded Dst_XY Registers

4-MByte region 1 (memory mapped regs)																											
256KByte sub-region 0																											
31		27		26		24		23		22		21		18		17 - 16		15		14		13		2		1 - 0	
00001				<GBASE>				0		1		0000				0 - 1		<Cmd>				<Count>				1 - 0	

13.7. DRAWING ENGINE REGISTERS

The software controls the graphic drawing by writing to the GE registers to set-up and initiate an operation. Any data that must be provided by the host is written to the Data_port. The Data_port can be referenced via the Data_port "register" or via the 4 MB window of aliases.

All registers can be read with accesses of any width. The CPU can read any register via Byte (8-bit), word (16-bit), or double-word (32-bit) accesses.

A register that is exclusively for the use of software, "Xtra", is included in the GE but has no influence on any drawing operation or on the display.

13.8. REGISTER ACCESS

Except for the Dst_XY register, discussed in the previous section, the memory-mapped GE registers and the Data Port are accessed by reading or writing to an address of the form. This is illustrated in [Table 13-6](#), where “Index” specifies the offset of the register to be accessed from the start of the GE memory-mapped register address space. The least significant two bits of Index will always be ‘00’. The following sections will list the “Index” value along with a description of each register. Reads may be done in any width, but writes must be done as 32-bit or 64-bit transfers.

In general, the CPU should not write to any of the GE registers when the GE is busy. If such an access is done, the CPU may be held for a long period of time, possibly for the duration of a large BitBlt. Reads of GE registers (except for Status) may return invalid data if the GE is busy.

The Dst_XY, Src_XY, Width and Height registers are double buffered and the CPU may write the next values to these registers while a prior operation is being performed. The last write to any double buffered register done before a write to Dst_XY will be the one used for the next operation. Any writes done to a GE register after a write is done to the Dst_XY while the GE is busy will hold the CPU until the first operation is completed and the pending register values are used for the second operation. During normal operation, the CPU writes to the Dst_XY register for text and line segments, reducing the hold period as much as possible.

The GE Status register may be accessed at any time.

13.8.1. DATA PORT ACCESS

The CPU writes Host data to the GE through the Data Port for Text and Host-to-screen BitBlt operations. The Data Port appears as one of the registers, as discussed in the previous section. Behind the Data Port, the Data FIFO buffers incoming data from the CPU. The Data Port is also repeatedly aliased in the upper 4 MBytes of the GE 16 MByte address space.

In normal operation for text drawing (done as a bitmap expanded Host-to-screen BitBlts), the CPU writes exact amount of data to the Data Port for the current character, then starts on the next text character by writing to the Dst_XY register and finally writes data for the next text character. The current operation reads from the Data Port FIFO until its needs are met. Then the next BitBlt operation reads its data from the Data Port FIFO. To ensure correct results, the software must write the correct number of 32-bit double words to the Data Port FIFO for all BitBlt operations.

The CPU can write to the Data Port at any time. If the GE is unable to accept any additional writes to the Data Port, the CPU is held off until the write command can be accepted. If a PCI master requests bus access when the CPU has been held off for a long period of time (128 clocks cycles), then the GE forces a CPU retry via the backoff (BOFF) mechanism.

Table 13-6. GE and Data_Port Access

4-MByte region 1 (memory mapped regs)											
256KByte sub-region 0											
31	27	26	24	23	22	21	18	17	12	11	0
00001		<GBASE>		0 - 1		0000		000000		<Index>	

GRAPHICS ENGINE

13.9. REGISTER SPECIFICATION

The GE registers are listed in alphabetical order and defined below.

13.9.1. BACKGROUND COLOUR REGISTER

This register contains the full-colour value(s) that a '0' bit is expanded to. This expansion is done for BitBlt operations with bitmap expansion specified in the Expand field of the ROP register, and for operations with the Source field of the ROP register set to CONSTANT_FILL.

For 8-bit pixels, only bits 7-0 are significant. For 16-bit pixels, only bits 15-0 are significant. For 24-bit pixels, only bits 23-0 are significant.

Background								Access = GBASE+400000h				Regoffset = 0x004h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BC															
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BC															
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-0	BC	Background Colour. This is the colour to be used as the background when expanding bitmap '0' values or when using CONSTANT_FILL as the source operand.

Programming notes:

The content of this register is not altered by drawing operations.

13.9.2. CURSOR COORDINATE REGISTER

This register contains the address of the upper-left-hand corner of the cursor. To eliminate the cursor, its address should be set to a value large enough so that none of the cursor is on the displayed screen. Note that when set to (0,0), the entire cursor may be displayed on the upper-left hand corner of the display.

Cursor_XY				Access = GBASE+400000h								Regoffset = 0x11Ch			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv			CYUL												
Default value after reset = undefined															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv			CXUL												
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-29	Rsv	Reserved.
Bits 28-16	CYUL	CYUL . The Y location of the upper-left-hand corner of the cursor.
Bits 15-13	Rsv	Reserved.
Bits 12-0	CXUL	CXUL . The X location of the upper-left-hand corner of the cursor.

Programming notes:

To suppress cursor display, enter one more than the number of display scan lines into the Y field.

The contents of this register remain unaltered throughout drawing and display operations.

GRAPHICS ENGINE

13.9.3. TOP OF DATA FIFO REGISTER

This write-only register is the port through which the CPU provides Host data.

Data_Port																Access = GBASE+400000h																Regoffset = 0x804h																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	DP																																
Default value after reset = undefined																																																

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DP															
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-0	DP	Data_Port.

Programming notes:

The CPU can write to the Data Port at any time. If the GE is unable to accept any additional writes to the Data Port, the CPU will be held off until the write can be accepted.

Note that writing to this address is the same as writing to any double word between:

(128 MBytes+(GBASE << 24) + 12 MBytes) to (128 MBytes+(GBASE << 24) + 16 MBytes).

The Data FIFO is empty after reset.

13.9.4. DESTINATION OPERAND BASE ADDRESS REGISTER

This register specifies the starting DRAM linear address of the destination operand (aligned to a 32 Byte boundary).

Dst_Base						Access = GBASE+400000h						Regoffset = 0x018h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv											DOB				
Default value after reset = undefined															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DOB															
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-21	Rsv	Reserved.
Bits 20-0	DOB	DstOp_Base. Base DRAM linear address of the destination operand with 16 Byte alignment. Lower five Bytes are reserved and are set to '0'.

Programming notes:

The contents of this register are not altered by drawing operations.

GRAPHICS ENGINE

13.9.5. DESTINATION PITCH REGISTER

This register specifies the number of Bytes needed to advance from a pixel in one scan line of the Destination to the corresponding pixel in the next scan line. This value is always positive. The Y_dirfield of the Pixel_depth register controls how the operation advances to the next scan line.

Only a limited number of pitches are supported. The supported ones (in Bytes) are listed in the Src_pitch description.

This register can be accessed via 32-bit or 16-bit transfers.

Dst_Pitch Access = GBASE+400000h Regoffset = 0x028h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv															
Default value after reset = undefined															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv					DS3		DS2			DS1			DS0		
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-11	Rsv	Reserved.
Bits 10-9	DS3	Dst_shift3. These bits specify an amount to multiply Dst_XY.Y, this result along with the other shift results, is added to the Dst_base and Dst_XY.X to compute the DRAM linear address of the destination pixel. See Table 13-7 for the multiplication values that this field can specify.
Bits 8-6	DS2	Dst_shift2. See Dst_shift3, above.
Bits 5-3	DS1	Dst_shift1. See Dst_shift3, above.
Bits 2-0	DS0	Dst_shift0. See Dst_shift3, above.

Table 13-7. DRAM Address Multiplication Factor

Value	Shift0	Shift1	Shift2	Shift3
000	0	0	0	0
001	0	0	32 * Y	1024 * Y
010	0	64 * Y	64 * Y	2048 * Y
011	128 * Y	128 * Y	128 * Y	4096 * Y
100	256 * Y	256 * Y	256 * Y	n/a
101	512 * Y	512 * Y	512 * Y	n/a
110	1024 * Y	1024 * Y	0	n/a
111	2048 * Y	0	0	n/a

Programming notes:

The contents of this register are not altered by drawing operations.

Journal of Management Inquiry 20(6) 798-814

[illegible]

Dst_XY				Access = GBASE+400000h								Regoffset =			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DY															
Default value after reset = undefined															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DX															
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-16	DY	Dst_Y . The unsigned Y coordinate of the starting corner of the destination operand.
Bits 15-0	DX	Dst_X . The unsigned X location of the starting corner of the destination operand. This value must be a multiple of Pixel_depth. The complete addressing of this register is described in Section 13.6.1 . "Command Initiation".

○ ○

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

[illegible]

GRAPHICS ENGINE

13.9.7. FOREGROUND COLOUR REGISTER

This register contains the full-colour value(s) that a “1” bit is expanded to.

Foreground				Access = GBASE+400000h								Regoffset = 0x034h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FCI															
Default value after reset = FFFFFFFFh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FCI															
Default value after reset = FFFFFFFFh															

Bit Number	Mnemonic	Description
Bits 31-0	FCI	Frg_CI. This is the colour to be used as the foreground when expanding bitmap ‘1’ values.

:

Programming notes:

This expansion is done for BitBlt operations with bitmap expansion specified in the Expand field of the ROP register.

For 8-bit pixels, only bits 7-0 are significant. For 16-bit pixels, only bits 15-0 are significant. For 24-bit pixels, only bits 23-0 are significant.

The contents of this register are not altered by drawing operations.

Height Access = GBASE+400000h Reqoffset = 0x048h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H															
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-16	Rsv	Reserved.
Bits 15-0	H	Height. The value set in these bits must be one less than the height, in scan lines, of the source and destination areas.

This register can be accessed via 32-bit or 16-bit transfers.

This register can be loaded by writing to the Dst_XY register using one the Height-specified address alias. For this case, the Height register is loaded with the value in the Count field of the address described in 13.6.1. "Command initiation".

This register is double-buffered. While the GE is busy executing one operation, a new value may be safely written to this register for the next operation. If the Dst_XY double-buffered register is full, then the CPU will be held off. This feature is specifically implemented to accelerate the Text and Line Segment operations.

The contents of this register are not altered by drawing operations.

GRAPHICS ENGINE

13.9.9. PATTERN BASE ADDRESS OPERAND REGISTER

This register contains the starting DRAM linear address of the Pattern operand, including the aligned base address, the first row to be displayed and a starting Byte number for 24-bit pixels.

Pattern										Access = GBASE+400000h					Regoffset = 0x058h				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Rsv										PB									
Default value after reset = undefined																			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PB								Rsv			PXS		Rsv		
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-22	Rsv	Reserved.
Bits 21-8	PB	Pattern base. These bits specify the starting DRAM physical address of the Pattern, operand, aligned to a 256 Byte boundary.
Bits 7-5	Rsv	Reserved.
Bits 4-3	PXS	Pat_X_start. For 24-bit pixels, these bits must be set to: (Dst_X / 8) modulo 3 where Dst_X is the Byte address of the first 24-bit pixel in the destination row. For all other pixel depths, the values must be set to "00".
Bits 2-0	Rsv	Reserved.

Programming notes:

The start of Pattern data must be aligned to a 256-Byte boundary. Advancing to the next Pattern data row will be done modulo 8 rows. Regardless of the number of Pixel_depth, the Pattern row is 32 Bytes long.

The Pattern register can be loaded with the address of the last row of Pattern data and the GE will wrap-around to the start of the pattern on the second row. Note that the Pattern register advances by increasing the address regardless of the X_dir, Y_src_dir or Y_dst_dir fields of the Pixel_depth register.

For further discussion of the Pattern Data, see [Section 13.10.1. "Pattern Data"](#).

The contents of this register are not altered by drawing operations.

13.9.10. PIXEL DEPTH OPERAND REGISTER

This register contains the number of Bytes in a pixel, and bits that control the direction of Screen-to-screen BitBlts.

Pixel_Depth								Access = GBASE+400000h				Regoffset = 0x07Ch			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv															
Default value after reset = undefined															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv								Y	Y	X	Rsv			PD	
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-8	Rsv	Reserved.
Bit 7	Y	Y_src_dir. When this bit is set to '0', source pixels advance from upper scan lines to lower scan lines (from smaller linear to larger linear addresses). Setting this bit to '1' reverses the direction of BitBlt source operations. This bit should be set to '0' for all operations other than reverse-direction non-bitmap-expanded screen-to-screen BitBlts.
Bit 6	Y	Y_dst_dir. When this bit is set to '0' destination pixels advance from upper scan lines to lower scan lines (from smaller to larger linear addresses). Setting this field to '1' reverses the direction of BitBlt destination operations. This field should be set to '0' for all operations other than reverse-direction non-bitmap-expanded screen-to-screen BitBlts.
Bit 5	X	X_dir. When this bit is set to '0', pixels advance from left to right, and when set to '1' they advance from right to left. This field can be set to '1' only for Screen-to-screen BitBlts and horizontal scan line fills.
Bits 4-2	Rsv	Reserved.
Bits 1-0	PD	Pixel depth. The only supported values for this field are shown in Table 13-8 .

Table 13-8. Supported Pixel Depth Values

Bit 1	Bit 0	Pixel Depth
0	0	1 Byte per pixel
0	1	2 Bytes per pixel
1	0	3 Bytes per pixel
1	1	4 Bytes per pixel

GRAPHICS ENGINE

Programming notes:

Note that the fourth Byte of 4-Byte pixels is not used in the display, but is processed by drawing operations. Zeros should be written to this 4th Byte to preserve compatibility with future versions of this architecture.

This register can be accessed via 32-bit or 16-bit transfers.

The contents of this register are not altered by drawing operations.

13.9.11. RASTER OPERATION REGISTER

This register contains the ROP code to be applied to process a pixel, to enable bitmap expansion, to select transparent modes, and to control the source operand. This is summarised in [Table 13-9](#).

ROP					Access = GBASE+400000h							Regoffset = 0x08Ch			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S		P	D	DM	Rsv										
Default value after reset = undefined															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D	D	S	S	P	E	P	B	R							
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-30	S	Source. These bits determine the SRC operand. Possible values are shown in Table 13-10 . This field MUST be set to CONSTANT_FILL if the Raster Operation requires no SRC operand (such as in inverting the destination as well as constant fills). Failure to set this field correctly can result in a degradation of performance. Note that CPU writes to the Data Port will complete without error, and the data will be ignored unless the Source field is set to HOST.
Bit 29	P	PAT present. This bit is set to '1' if a pattern data is to be used during the operation.
Bit 28	D	DST present This bit is set to '1' if destination data is to be read during the operation.
Bit 27	DM	Diagnostic Mode. For normal operation this bit should be set to '0'. When set to '1', GE register reads will be done from an alternative path for diagnostic verification.
Bits 26-16	Rsv	Reserved.
Bit 15	D	DST transparency mode. When this is set to '1', pixels are selectively modified based upon a comparison of the DST data from the frame buffer vs. the DST transparency compare register. The results of the comparison are interpreted based upon the DST transparency match bit. Note that the DST present bit must also be set to '1' when this bit is set. This mode is not valid when the pixel depth is 3 Bytes per pixel.
Bit 14	D	DST transparency match. This mode applies only when DST transparency mode is set. When this bit is set to '1', pixels with DST data that match the DST transparency compare register will be modified. When it is set to '0', pixels with DST data that do not match the DST transparency compare register will be modified.

GRAPHICS ENGINE

Bit Number	Mnemonic	Description
Bit 13	S	SRC transparency mode. When this is set to '1', pixels are selectively modified based upon a comparison of the SRC data vs. the SRC transparency compare register. The results of the comparison are interpreted based upon the SRC transparency match bit. This mode is only meaningful when using non-bitmap screen or host data as the source. Transparency for bitmap source data should not use this mode, but rather the SRC bitmap transparency mode. This mode is not valid when the pixel depth is 3 Bytes per pixel.
Bit 12	S	SRC transparency match. Applies only when SRC transparency mode is set. When this bit is set to '1', pixels with SRC data that match the SRC transparency compare register will be modified. When this is set to '0', pixels with SRC data that do not match the SRC transparency compare register will be modified.
Bit 11	P	Packed. If set to '1', the source will be read in packed mode. Effectively, the source is viewed as a continuous stream of data. At the end of a destination scan line, any data remaining in the last-used source Dword is applied to the start of the next destination scan line. When this bit is set to '0', any remaining source data is discarded at the end of a destination scan line. New source data is read from the next source scan line to apply to the start of the next destination scan line.
Bit 10	E	Expand. If set to '1', the bitmap expansion will be enabled and source data from screen or host is assumed to be bitmap data. If set to '0', source data is assumed to be colour data with the depth specified in the Pixel_depth register.
Bit 9	P	PAT transparency mode. When this bit is set to '1', pixels are selectively modified based upon the value of corresponding pattern data. Pattern Bytes that are set to zero are not modified. Note that the PAT present bit must also be set to '1' when this bit is set.
Bit 8	B	Bitmap transparency mode. When this bit is set to '1', pixels are selectively modified based upon the pre-expanded bitmap value. Pixels with corresponding bitmap values of zero are not modified. Pixels with corresponding bitmap values of one are written with the foreground value. Note that the expand bit must also be set when using this mode.
Bits 7-0	R	ROP , the raster operation used when computing a pixel result value.

Table 13-9. Summary of ROP Functions

Bits	Function
31:30	SRC operand type
29	Use PAT operand
28	Use DST operand
27	GE Diagnostic mode
26:16	Unused/Reserved
15	DST transparency mode
14	DST transparency match
13	SRC transparency mode
12	SRC transparency match
11	Packed SRC data
10	SRC bitmap expansion
9	PAT transparency mode
8	SRC bitmap transparency
7:0	Raster operation code

Table 13-10. Detail of SRC Operand Functions

Bit 31	Bit 30	Function	Source
0	0	CONSTANT_FILL	Background colour register
0	1	SCREEN	screen or frame buffer
1	0	HOST	host CPU
1	1	Reserved	

Programming notes:

The contents of this register are not altered by drawing operations.

GRAPHICS ENGINE

13.9.12. SOURCE BASE ADDRESS OPERAND REGISTER

This register specifies the starting DRAM linear address of the source operand (aligned to a 32-Byte boundary).

Src_Base							Access = GBASE+400000h					Regoffset = 0x098h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv										SB					
Default value after reset = undefined															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SB											Rsv				
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-22	Rsv	Reserved.
Bits 21-5	SB	SrcOp_Base. Base linear address of the source operand.
Bits 4-0	Rsv	Reserved. These bits are set to '0'.

Programming notes:

The contents of this register are not altered by drawing operations.

13.9.13. SOURCE PITCH OPERAND REGISTER

This register specifies the number of Bytes needed to advance from a pixel in one scan line of the source to the corresponding pixel in the next scan line. This value is always positive. The Y_src_dir field of the Pixel_depth register controls how the operation advances to the next scan line.

Only a limited number of pitches are supported. The supported pitches (in Bytes) are described in [Section 13.6. "VGA operand frame buffer addresses"](#).

Src_Pitch					Access = GBASE+400000h								Regoffset = 0x0ACh			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Rsv																
Default value after reset = undefined																

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv					S3		S2			S1			S0		
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-11	Rsv	Reserved.
Bits 10-9	S3	Src_shift3 . These bits specify an amount to multiply Src_XY.Y, this result along with the other shift results, is added to the Src_base and Src_XY.X to compute the DRAM linear address of the source pixel. See the Table 13-11 . below for the multiplication values that this field can specify.
Bits 8-6	S2	Src_shift2 . See Src_shift3, above.
Bits 5-3	S1	Src_shift1 . See Src_shift3, above.
Bits 2-0	S0	Src_shift0 . See Src_shift3, above.

Table 13-11. Scr_shift3 Multiplication Factors

Value	Shift0	Shift1	Shift2	Shift3
000	0	0	0	0
001	0	0	32 * Y	1024 * Y
010	0	64 * Y	64 * Y	2048 * Y
011	128 * Y	128 * Y	128 * Y	4096 * Y
100	256 * Y	256 * Y	256 * Y	n/a
101	512 * Y	512 * Y	512 * Y	n/a
110	1024 * Y	1024 * Y	0	n/a
111	2048 * Y	0	0	n/a

Programming notes:

This register can be accessed via 32-bit or 16-bit transfers. The contents of this register are not altered by drawing operations.

GRAPHICS ENGINE

13.9.14. SOURCE COORDINATE REGISTER

This register contains the coordinate address of the starting corner of the source operand.

Src_XY				Access = GBASE+400000h								Regoffset = 0x0BC h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SY															
Default value after reset = undefined															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SX															
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-16	SY	Src_Y. The source operand starting corner of the unsigned Y coordinate.
Bits 15-0	SX	Src_X. The source operand starting corner of the unsigned X location. When bitmap expansion is not enabled, this is a Byte address. When in bitmap expansion is enabled, this is a bit address.

Programming notes:

The “starting” corner is controlled by the X_dir and Y_src_dir fields of the Pixel_depth register.

This register is double-buffered. While the GE is busy executing one operation, a new value may be safely written to this register for the next operation. If the Dst_XY double-buffered register is full, then the CPU will be held off.

The Y field and all but the lower three bits (five when bitmap expansion is enabled) of the X field are ignored during Host-to-screen BitBlts.

The contents of this register are not altered by drawing operations.

13.9.15. STATUS REGISTER

Status		Access = GBASE+400000h										Regoffset = 0x908h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GB	PB	Rsv													
0		Default value after reset = undefined													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv															
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bit 31	GB	GE_Busy. This read/write bit is set to '1' when the GE is busy, GE register accesses that are done when this bit is set may result in the CPU being held for the duration of the current operation.
Bit 30	PB	Pending Busy. This read-only bit is set to '1' when the Dst_XY pending register has data in it. If GE writes to that registers when this bit is set it may result in the CPU being held for the duration of the current operation. GE register reads always return data without holding the CPU, but the data returned from the read may not be valid. The Status register may be read at any time and the operation will return valid data. Note that Pending Busy implies Busy, that is the Pending Busy field can be set to '1' only if the Busy field is also set to '1'.
Bits 29-0	Rsv	Reserved. These may read as one or zero.

Width						Access = GBASE+400000h						Regoffset = 0x0C8h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv															
Default value after reset = undefined															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W															
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-16	Rsv	Reserved.
Bits 15-0	W	Width. These bits should be set to one less than the number of Bytes across the destination area. This value should be a multiple of Pixel_depth, because only the number of Bytes specified in this field will be modified.

13.9.17. EXTRA USE REGISTER

This register contains 32 bits of data that software can read from and write to.

This register has no effect on any drawing operation or display.

Xtra				Access = GBASE+400000h								Regoffset = 0x0D4h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
D															
Default value after reset = undefined															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D															
Default value after reset = undefined															

Bit Number	Mnemonic	Description
Bits 31-0	D	Data for user software use.

Programming notes:

The contents of this register are not altered by drawing operations.

GRAPHICS ENGINE

13.9.18. SRC TRANSPARACENCY COMPARE REGISTER

This 32-bit register contains the pixel value used for comparison in SRC transparency mode. For pixels depths of one Byte per pixel, the pixel value must be replicated in all four Bytes of this register. For pixel depths of two Bytes per pixel, the pixel value must be replicated in the upper and lower 16 bits of this register.

SRC_Transparency								Access = GBASE+400000h								Regoffset = 0xEC							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16								
D								C															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
B								A															

1 byte per pixel	colour replicated in A, B, C and D
2 bytes per pixel	colour replicated across A, B and C, D
3 bytes per pixel 24-bit colour	colour replicated across A, B and C
4 bytes per pixel 32-bit colour	colour replicated across A, B, C and D



13.9.19. DST TRANSPARENCY COMPARE REGISTER

This 32-bit register contains the pixel value used for comparison in DST transparency mode. For pixels depths of one Byte per pixel, the pixel value must be replicated in all four Bytes of this register. For pixel depths of two Bytes per pixel, the pixel value must be replicated in the upper and lower 16 bits of this register.

DST_Transparency

Access = GBASE+400000h

Regoffset = 0xFCCh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
D								C							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B								A							

1 byte per pixel	colour replicated in A, B, C and D
2 bytes per pixel	colour replicated across A, B and C, D
3 bytes per pixel 24-bit colour	colour replicated across A, B and C
4 bytes per pixel 32-bit colour	colour replicated across A, B, C and D

GRAPHICS ENGINE

13.9.20. NOTES ON: INTERACTIONS BETWEEN BLT OPERATIONS AND VGA FRAMEBUFFER ACCESSES

The GE performs two major classes of operations: BitBlts and standard VGA Framebuffer accesses. These two types of operations share resources in the hardware. This imposes certain requirements on driver software.

The state of all standard VGA registers is unchanged by BitBlt and extended register reads/writes with the exception of the CR22 data latch. The state of this register is undefined after a BitBlt.

The state of all extended registers is unchanged by VGA read/write operations.

Between a BitBlt operation and a VGA read/write operation, the software must ensure that no BitBlt operation is in progress by means of the Status register.

Before performing any VGA read/write operations, the software must ensure the Foreground register has the value FFFFFFFFh and the background register has the value 00000000h. These are also the reset values of these registers.

Between a VGA write operation and a BitBlt operations, the software must ensure the VGA write pipeline is flushed by performing a VGA read operation.

13.10. GE OPERATIONS

13.10.1. PATTERN DATA

If the ROP register value specifies that pattern data is used in the computation of the destination results, then one row of the pattern data is read at the start of each scan line processed. This row of data is repeatedly applied to the result computation across scan line. The Pattern register points to the start of an 8-pixel-by-8-pixel colour area that is aligned to the destination. The GE does not perform any horizontal alignment to the pattern data.

When the pixel depth is three Bytes, the least significant three bits of the Pattern register must indicate which Byte starts the pattern row. This field should be set to:

$$(\text{Dst_X} / 8) \text{ modulo } 3$$

where Dst_X is the Byte address of the first 24-bit pixel in the destination row. (The same value that is written to the X field of the Dst_XY register).

Bitmap patterns are not directly supported. To use a bitmap pattern, first allocate off-screen frame buffer memory for a colour version of the pattern. Then set up the GE to perform a Host-to-screen BitBlt with bitmap expansion into this allocated memory. The bitmap pattern is then written to the Data Port. The expanded pattern can now be used by pointing the Pattern register to the allocated memory.

13.10.2. BITMAT CONSIDERATIONS

Screen-to-screen and Host-to-screen operations can optionally expand single-bit-per-pixel bitmaps into colour pixels. Each '1' bit is replaced by the contents of the Foreground colour register and each '0' bit is replaced by the contents of the Background colour register.

Bitmaps from the frame buffer (during Screen-to-screen BitBlts) must be aligned on a quad-word (64-bit) boundary. Bitmaps from the Host can be aligned on a double-word (32-bit) boundary. Leading bits of the bitmaps may be skipped by setting the least significant bits of the X field of the Src_XY register to the number of bits in the Byte to be ignored. When in bitmap expansion mode, the X field of the Src_XY address can be thought of as a bit address instead of a Byte address. For Host-to-screen bitmap expanded BitBlts only the least significant five bits of the Src_XY.X register are significant. The first bit after those skipped will then be aligned to the first destination pixel.

For bitmap expansion, the X_dir must be '0'. The result for a bitmap expansion BitBlt with X_dir set to '1' is not defined.

With the X_dir field of the Pixel_depth register set to '0', the bitmap is considered to start at the least significant end of the first quad-word and continues towards the most significant end of the quad-word and then to higher memory addresses. The first bit of a quad-word is bit 7 of Byte 0 and the last bit is bit 0 of Byte 7.

13.10.3. BITBIT OPERATIONS

Using the GE's BitBlt commands it is possible to implement the following six operations:

- 1) Rectangular Fill
- 2) Screen-to-screen BitBlt
- 3) Host-to-screen BitBlt
- 4) Packed Text
- 5) Microsoft Font Text
- 6) Line Segments

13.10.4. RECTANGULAR FILL

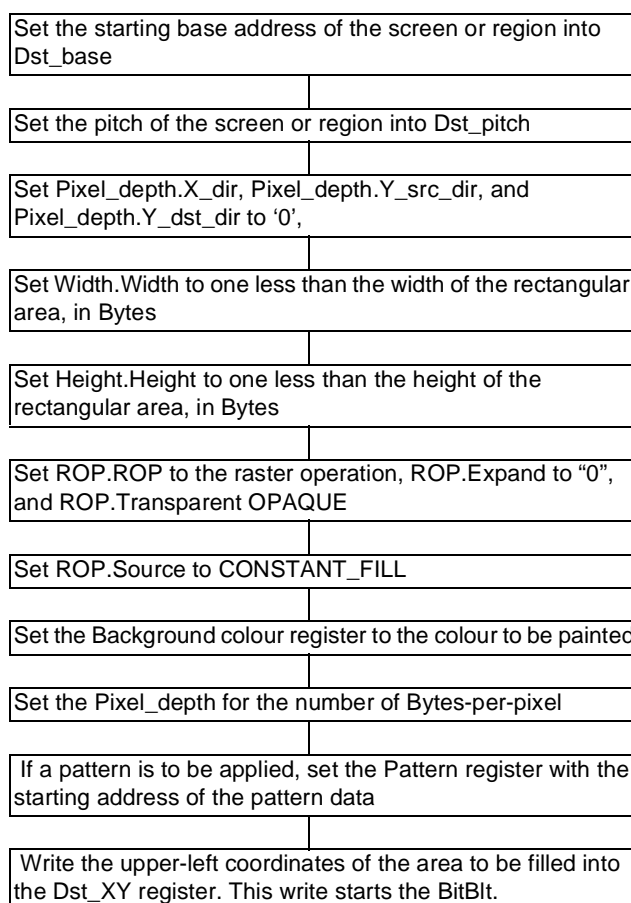
A rectangular fill operation is used to fill rectangular areas in the frame buffer with solid or patterned colours. The function performed during the fill operation is:

ROP ((Background), (Pattern), (Destination)) -> (Destination)

The specified rectangle is filled with the contents of the Background colour register, the pattern data and the existing destination contents, as modified by the ROP. The CPU provides the rectangle upper-left (Dst_XY) coordinates, the width and the height of the rectangle. Destination and pattern data can be anywhere in the frame buffer. ROP may be any of the 256 standard raster operations.

The Rectangular Fill operation is optimised to run at the memory bandwidth.

To perform a rectangular fill (except for the last write, order is unimportant):



Frequently, some of these parameters will already be set up from prior operations, such as Dst_pitch, Background colour, and Pixel_depth. These will not need to be written each time.

The implementation of this operation is performance optimised and can drive the DRAM buffer at full bandwidth. Thus, resulting pixels are computed in groups of 32 bits, to allow one 64-bit result every two

video domain clock cycles. As the memory subsystem supports separate Byte-write enables, the first and last 64-bit write in each scan line can be performed without requiring a read-modify-write cycle.

13.10.5. SCREEN-TO-SCREEN BITBIT

The Screen-to-screen BitBlt operation is used to copy data from one rectangle in the frame buffer (either on-screen or off-screen areas) to another with the identical geometry. The pixel depth of the source region must match that of the destination region, or it may be a bitmap (if bitmap expansion is specified by setting ROP.Expand).

The function performed during the BitBlt operation is:

ROP ((Source), (Pattern), (Destination)) -> (Destination)

If these rectangular areas are overlapping, then the direction of the BitBlt must be carefully selected:

** Source region is below the destination:*

- > BitBlt should be done from the upper-left-hand corner and progress downwards,
- > the X_dir, Y_src_dir and Y_dst_dir fields of the Pixel_depth register should be "0".

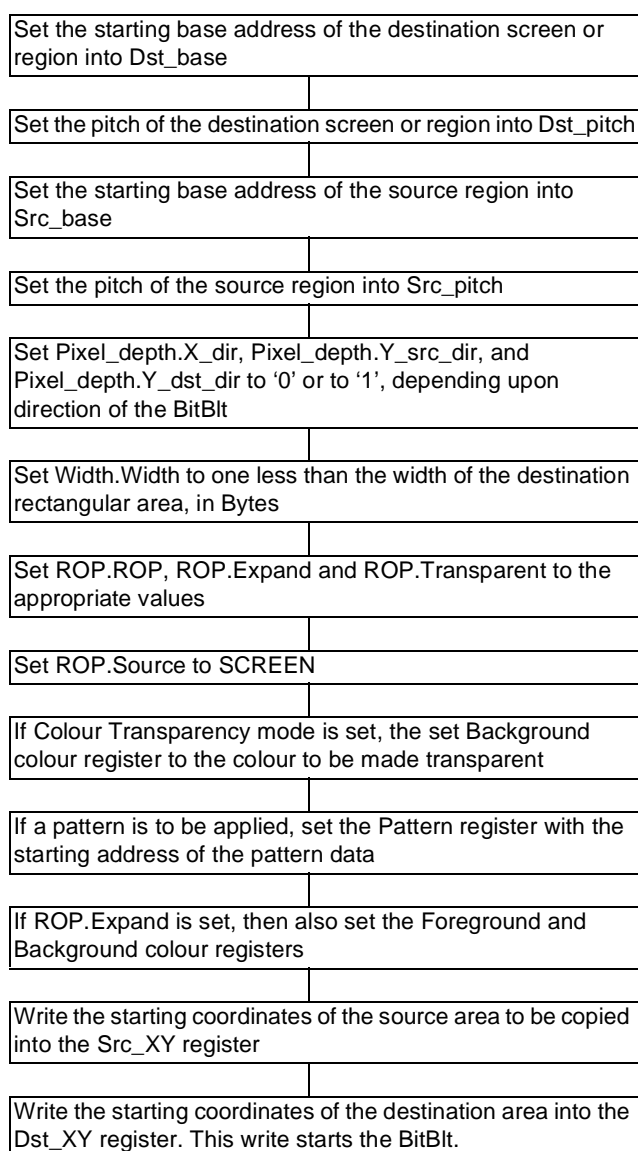
** Source region is above the destination:*

- > BitBlt should be done from the lower-right-hand corner and progress upwards,
- > the X_dir, Y_src_dir and Y_dst_dir fields of the Pixel_depth register should be "1".

The Source, destination and pattern data can be anywhere in the frame buffer. The ROP may be any one of the 256 standard raster operations.

GRAPHICS ENGINE

To perform a Screen-to-screen BitBlt (except for the last write, order is unimportant):



Frequently, some of these parameters will already be set up from prior operations, such as Dst_pitch, Foreground colour, Background colour, and Pixel_depth. These will not need to be written each time.

The implementation of this operation is performance optimised and can drive the DRAM buffer at full bandwidth during constant fills. Thus, resulting pixels are computed in groups of 32 bits, to allow one 64-bit result every two graphics clock domain cycles. As the memory subsystem supports separate Byte-write enables, the first and last 64-bit write in each scan line can be performed without requiring a read-modify-write cycle.

13.10.6. HOST-TO-SCREEN BITBIT

The Host-to-screen BitBlt is used to copy data from the Host CPU to the frame buffer (either on-screen or off-screen areas). Note that if the CPU has built a rectangle in the frame buffer memory area with the Host data, then the Screen-to-Screen BitBlt operation can be used instead of this operation.

The pixel depth of the Host data must match that of the Destination region, unless it is a bitmap (if bitmap expansion is specified).

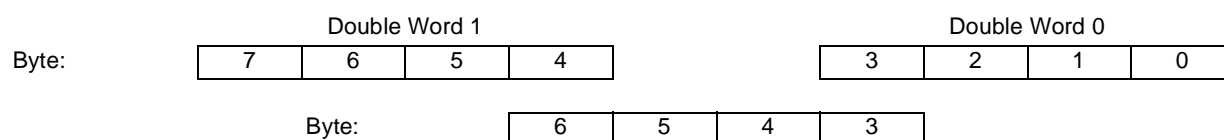
The function performed during the BitBlt is:

ROP((Host),(Pattern),(Destination))->(Destination).

The host area data is supplied by the CPU, which writes its data into the Data Port. The destination and pattern data can be anywhere in the frame buffer.

ROP may be any one of the 256 standard raster operations.

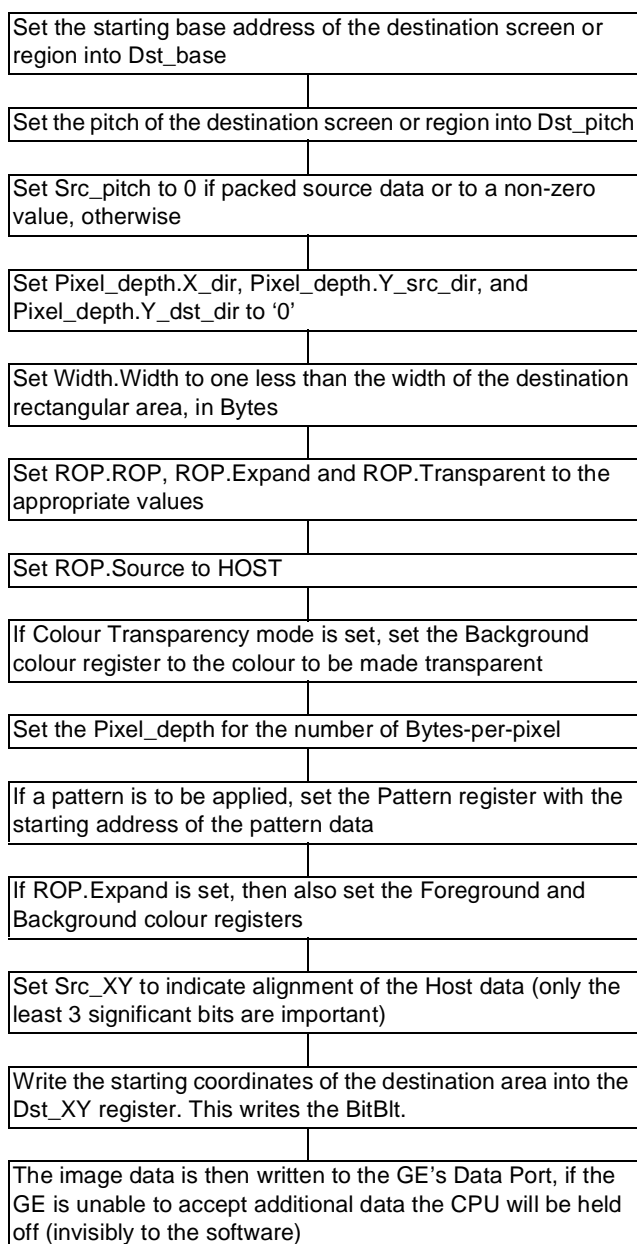
The CPU specifies the number of least significant Bytes of the first double-word that should be discarded, via the least significant three bits of the X field in the Src_XY register. The GE then merges Bytes of two double-words at a time, in order to build a double-word to operate on. For example, if the X field was set to 3, then the last Byte of the first double-word and the first three Bytes of the second double-word would be combined to form the first Host data double-word:



The CPU must provide the number of words required for Height * Width pixels. At the end of a scan line, the GE will discard the excess Host Bytes or bits that may be left in the last double-word and advance to the next scan line, unless Src_pitch is set to 0. In this case, data for adjacent scan lines are contiguous in the host data stream.

GRAPHICS ENGINE

To perform a Host-to-screen BitBlt (except for the last write, order is unimportant):



Frequently, some of these parameters will already be set up from prior operations, such as Dst_pitch, Foreground colour, Background colour, and Pixel_depth. These will not need to be written each time.

13.10.7. PACKED TEXT

The Packed Text operation is used to efficiently expand packed bitmap fonts into full colour representations in the frame buffer (either on-screen or off-screen areas). This operation is implemented as a Host-to-screen BitBlt with bitmap expansion and packed source data. The next section discusses how to handle Microsoft Font Text operations.

The function performed during the Packed Text operation is:

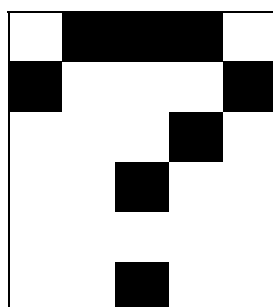
ROP ((Host), (Pattern), (Destination)) -> (Destination).

The Host packed bitmap data is supplied by the CPU via writes to the Data Port and is organised as double-words containing 32 bits of information. Each bit corresponds to a pixel. This data is expanded into Background and Foreground colours, unless the bitmap expansion transparent mode is on. If the transparent mode is set, then Host data bits of '0' suppress any changes to the corresponding destination pixels. The Destination and Pattern can be anywhere in the frame buffer.

ROP may be any one of the 256 standard raster operations.

In a standard bitmap, the start of each scan line is aligned to a pitch-specified boundary. This is acceptable for wide bitmaps, however text font bitmaps are usually not very wide. To increase the amount of information provided to the GE per Host write, the Text operands are bit-packed. Each 32-bit write contains only useful font data, except possibly for the trailing bits of the last write.

For example, question mark character might appear in a fictitious font as:



Or in Binary form:

0	1	1	1	0
1	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	0	0	0
0	0	1	0	0

This would appear in memory as in [Table 13-12](#).

In this example, the entire character bitmap fits into a single 32-bit double-word. This is a big saving when compared to having to send one 32-bit double-word for each font row. Note that two bits of don't cares exist at the (top) end of the double word. Since this character is five bits wide and six lines high, it only needs 30 bits of storage. The remaining two bits will not be displayed.

After setting up the registers, the CPU writes the Host data, in 32-bit quantities, to the Data Port.

GRAPHICS ENGINE

If a Pattern is applied to the text operation, a row of the pattern data will be read at the start of each character scan line.

Table 13-12. Bit Representation

top line						bottom line
01110	10001	00010	00100	00000		00100
Increasing memory addresses ----->						

Breaking this up into Bytes see [Table 13-13](#).

Table 13-13. Byte Representation

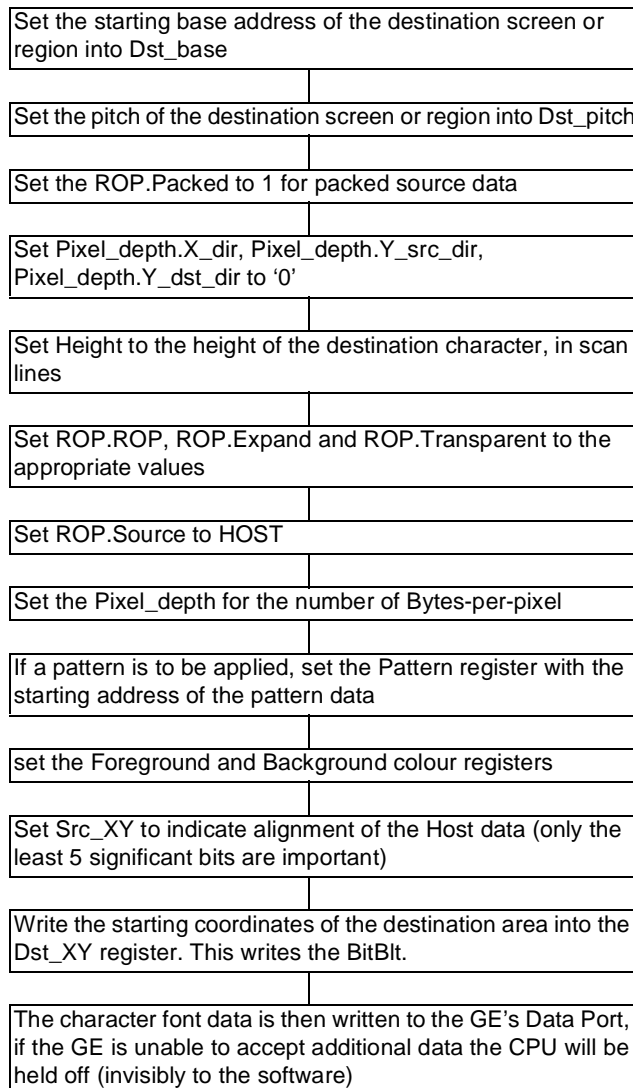
	01110100	01000100	01000000	000100XX
Byte	0	1	2	3

Breaking this up into a double-word as in [Table 13-14](#).

Table 13-14. Double Word Representation

	000100XX	01000000	01000100	01110100
	3	2	1	0
Byte				
Word		0		1

To perform a Packed Text BitBlt (except for the last write, order is unimportant):



To draw the next character, its starting address (taking into account inter-character spacing) is written to the Dst_XY register, along with that character's width encoded into the address of the Dst_XY register. This write can be done even if the GE is busy, as the Destination and Width registers are double buffered. The CPU then writes all the bitmap data that corresponds to the second character, the third Dst_XY/Width, the third bitmap data, etc.

Frequently, some of these parameters will already be set up from prior operations, such as Dst_pitch, Foreground colour, Background colour, and Pixel_depth. These will not need to be written each time.

13.10.8. MICROSOFT FONT TEXT

Microsoft fonts (consisting of 8-bit strips of a character) can be handled as simple 8-pixel-wide Host-to-screen BitBlts with bitmap expansion, but no packed data. The last strip of a character is handled in a different manner. The background colour for the last strip is first filled into its rectangular area. Then the strip data is drawn in transparent mode with the unused bits filled with zeros.

13.10.9. LINE SEGMENTS

The line segment operations are used to draw horizontal or vertical line segments. The segments are runs of pixels that start from a specified coordinate address (via the Dst_XY register) and whose length is specified in the address used when writing to the Dst_XY register.

The function performed during the line draw is:

ROP ((Background), (Pattern), (Destination)) -> (Destination)

ROP may be any one of the 256 standard raster operations.

Simple and complex curves can be efficiently drawn. The software on the CPU must generate all points or scan lines to be drawn and then use the GE to draw the line segments.

Two different types of line segments are supported: horizontal and vertical. For horizontal line segments, the Height register should be programmed to '0', to indicate a single pixel high line. The length of the line segment (in Bytes) will then be stored into the Width register when the Dst_XY register is written to (the length is encoded into the Count field of the Dst_XY register's address). For vertical lines, the Width register should be programmed to one less than the number of Bytes per pixel, to indicate a single pixel wide line. The length of the line segment is stored into the Height register when the Dst_XY register is written to.

It is possible to draw thicker line segments, by programming the Height register (for horizontal segments) or the Width register (for vertical segments) to other values.

For horizontal line segments, the X_dir, Y_src_dir and Y_dst_dir fields of the Pixel_depth register must be set to "0".

The Background colour register should be set to the colour of the line segment to be drawn.

13.11. CURSOR SUPPORT

The GE supports a 64x64x2 cursor. The cursor is actually two 64x64x1 arrays: an AND array and an XOR array. For any given pixel that is within the cursor's active region, the displayed pixel depends on the frame buffer pixel, the AND array value, the XOR array value and the Cursor_colour0 and Cursor_colour1 registers as shown in [Table 13-15](#).

The AND array is stored in off-screen memory, starting at Cursor. The XOR array is stored in off-screen memory starting at (Cursor + 512). Two 64-bit on-chip registers hold one scan line of each of these arrays. Before a scan line that possibly includes a cursor is displayed, these two registers are loaded from the appropriate off-screen locations.

Note that for 8-bit and 16-bit pixel depths, the above cursor operation is performed AFTER the data has been expanded by the colour look-up-table (LUT). Thus, the Inverted Frame Buffer Pixel is the complement of the full-colour pixel that would otherwise be displayed.

The cursor address (Cursor_XY) refers to the upper-left-hand corner of the cursor and specifies the distance, in pixels, from the upper-left-hand corner of the screen. So, if the cursor address were to be set to (0,0), then the entire cursor could be displayed in the upper-left-hand corner of the screen. The cursor active region thus may extend from:

(Cursor_XY.X, Cursor_XY.Y)

to

(Cursor_XY.X + 63, Cursor_XY.Y + height - 1)

as controlled by the Cursor Height register (CR29).

Note: To suppress cursor display, enter one more than the number of display scan lines into the Y field.

Table 13-15. Cursor Arrays

AND Value	XOR Value	Displayed Pixel
0	0	Cursor_colour0
0	1	Cursor_colour1
1	0	Frame Buffer Pixel
1	1	Inverted Frame Buffer Pixel

GRAPHICS ENGINE

13.11.1. CURSOR HEIGHT REGISTER (RW)

CR29

Access = 0x3X4h/0x3X5h

Regoffset = 029h

7	6	5	4	3	2	1	0
C XOR	CH						
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	C XOR	Cursor XOR Pre/Post Look Up Table. When this bit is set to one, the graphics cursor XOR operation is performed before the look up table. The default behaviour, when this bit is set to zero, is for the XOR operation to happen after the look up table. This is correct for 15, 16, 24 bit per pixel modes but not 8bpp.
Bits 6-0	CH	Cursor height. This field represents the vertical extent of the graphics cursor in scan lines. Setting this to zero effectively turns the graphics cursor off. Values greater than 40h (decimal 64) are meaningless and produce unpredictable results.

Programming notes:

There is no cursor width register - the width is always 64 pixels. If a narrower cursor is required, pad the bitmap on the right with transparent cursor colour (pad the AND plane with '1's on the right and the XOR plane with '0's).

13.11.2. CURSOR COLOUR 0 REGISTER A (RW)

CR2A			Access = 0x3X4h/0x3X5h			Regoffset = 02Ah	
7	6	5	4	3	2	1	0
CC 0 R							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	CC 0 R	Cursor Colour 0 Red. These bits are the red component of cursor colour 0.

GRAPHICS ENGINE

13.11.3. CURSOR COLOUR 0 REGISTER B (RW)

CR2B

Access = 0x3X4h/0x3X5h

Regoffset = 02Bh

7	6	5	4	3	2	1	0
CC 0 G							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	CC 0 G	Cursor Colour 0 Green. These bits are the green component of cursor colour 0.

13.11.4. CURSOR COLOUR 0 REGISTER C (RW)

CR2C

Access = 0x3X4h/0x3X5h

Regoffset = 02Ch

7	6	5	4	3	2	1	0
CC 0 B							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	CC 0 B	Cursor Colour 0 Blue. These bits are the blue component of cursor colour 0.

GRAPHICS ENGINE

13.11.5. CURSOR COLOUR 1 REGISTER A (RW)

CR2D

Access = 0x3X4h/0x3X5h

Regoffset = 02Dh

7	6	5	4	3	2	1	0
CC 1 R							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	CC 1 R	Cursor Colour 1 Red. These bits are the red component of cursor colour 1.

13.11.6. CURSOR COLOUR 1 REGISTER B (RW)

CR2E

Access = 0x3X4h/0x3X5h

Regoffset = 02Eh

7	6	5	4	3	2	1	0
CC 1 G							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	CC 1 G	Cursor Colour 1 Green. These bits are the green component of cursor colour 1.

GRAPHICS ENGINE

13.11.7. CURSOR COLOUR 1 REGISTER C (RW)

CR2F

Access = 0x3X4h/0x3X5h

Regoffset = 02Fh

7	6	5	4	3	2	1	0
CC 1 B							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	CC 1 B	Cursor Colour 1 Blue. These bits are the blue component of cursor colour 1.

13.11.8. GRAPHICS CURSOR ADDRESS REGISTER 0 (RW)

CR30

Access = 0x3X4h/0x3X5h

Regoffset = 030h

7	6	5	4	3	2	1	0
CAA							Rsv
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-1	CAA	Cursor AND Address Bits 15-9. These bits represent bits 15-9 of the DRAM linear address of the cursor's AND mask. The cursor's XOR mask begins at this address + 512. This memory must be aligned on a 1 KByte boundary. For a discussion of DRAM linear addresses, see Section 13.6 .
Bit 0	Rsv	Reserved. This bit should be written as zero.

Programming notes:

The cursor bitmap is ordered such that the top left hand corner of the cursor is represented by bit 7 of the Byte addressed by this field (AND) and bit 7 of the Byte at 512 plus this address (XOR plane). The next pixel right is represented by bit 6 of these Bytes and so on until the bottom right hand pixel is represented by bit 0 of the Byte located at this address plus 511 (AND) and bit 0 of the Byte at 1023 plus this address.

GRAPHICS ENGINE

13.11.9. GRAPHICS CURSOR ADDRESS REGISTER 1 (RW)

CR31

Access = 0x3X4h/0x3X5h

Regoffset = 031h

7	6	5	4	3	2	1	0
CAA							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0	CAA	Cursor AND Address Bits 23-16. These bits represent bits 23-16 of the DRAM linear address of the cursor's AND mask. For a discussion of DRAM linear addresses, see Section 13.6 .

13.11.10. GRAPHICS CURSOR ADDRESS REGISTER 2 (RW)

CR32			Access = 0x3X4h/0x3X5h			Regoffset = 032h	
7	6	5	4	3	2	1	0
Rsv					CAA		
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-3	Rsv	Reserved. These bits should be written as zero.
Bits 2-0	CAA	Cursor AND Address Bits 26-24. These bits represent bits 26-24 of the DRAM linear address of the cursor's AND mask. For a discussion of DRAM linear addresses, see Section 13.6 .

14. VIDEO INPUT PORT

14.1. INTRODUCTION

The STPC video input signals, buffering and TV output signals are managed by the Video Controller. The video input signal and buffering are controlled by the Video Input Port. This port interfaces with external digital video signals in various formats and is described in the remainder of this Chapter.

The TV Output Port, which controls the video TV output signal in various standard formats, is a high-performance PAL/NTSC TV digital encoder. This converts the digital video signal stream into a standard analog baseband PAL/NTSC TV signal, and also produces the RGB analog components. It supports both interlaced (525 and 625 line standards) and non-interlaced modes. The supported signal encoding formats include NTSC-M, PAL-B, D, G, H, I, N, M, plus NTSC-4.43 encoding. It can also perform Closed-Caption or CGMS encoding. The TV Output Port is described in the separate TV Output Port Chapter .

The video input and display signals are controlled through the Video Pipeline registers. These registers, which control the settings for the display buffer areas, plus filter control, colour mixing and colour space mixing, are described in the separate Video Pipeline Registers Chapter .

14.2. VIDEO INPUT PORT (VIP) OVERVIEW

The purpose of the Video Input Port is to accept an encoded digital video signal stream in one of a number of industry standard formats, decode it, optionally decimate it 2:1, and deposit it into an offscreen area of the Frame Buffer. An interrupt request can be generated when an entire field or frame has been captured.

The Video Input Port includes a fully functional VIP Host Master Port with hardware polling, programmable time-out period and programmable time-slice arbitration logic. This interface implements the full VIP Host Port Protocol - burst mode, master or slave-terminated transfers, wait-states and time-out transfers.

The channel has a 32-byte FIFO to optimise transfers to system memory while ensuring adequate bandwidth for VIP transfers. Both channels support Hardware Polling with a programmable delay period to reduce polling when the selected target FIFO is not ready. Hardware polling minimises the transfer start-up time for the DMA operations.

Arbitration between DMA Channels and host accesses can be round-robin or priority based. Round-robin arbitration and maximum burst length controls allow the maximum latency to be calculated and controlled. Priority based arbitration insures maximum bandwidth for critical tasks. The time-out period is programmable to accommodate devices with long access times.

14.3. DIGITAL VIDEO INPUT FORMATS

The video input port can be programmed to decode one of several video formats. The following sections discuss this functionality in more detail.

Existing video input formats are shown in [Table 14-1](#).

Table 14-1. Video Signal Formats

Input Format	Description
VIP 1.0 (ITU-R 656)	Lock internal timing generator to EAV codes
UTIR-601	8-bit multiplexed CCIR 601
Passthrough	Video stream is passed directly through the Video Ports without processing

VIDEO INPUT PORT

14.3.1. VIP 1.0 COMPATIBLE VIDEO

The Video Input Port supports the simplified SAV (Start of Active Video) and EAV (End of Active Video) codes, as defined in the VIP 1.0 Specification.

In this mode, the Video Timing Generator cannot be used to specify the horizontal or vertical active periods. The capture of video data must be based solely on the SAV and EAV codes embedded in the video stream.

This implementation includes:

- The Video Timing Generator used independently to generate the system timing signals HSYNC# and B/T#.
- Horizontal and vertical active window, based on SAV and EAV codes only.
- Byte swapping may be disabled, based on the Task Bit from the SAV code.
- Invalid pixel detection when the value is 0x00. When a pixel data value of 0x00 is encountered during an active line, the data is not written to the Frame Buffer and the pointer is not incremented. This allows re-sampled video to be output without changing the PIXCLK frequency.

14.3.2. 8-BIT MULTIPLEXED ITU-R 601

This mode provides a glueless video interface to the STi3520A MPEG-2 decoder chip. The video data interface consists of eight data pins, two control pins and a pixel clock. The UTIR-601 outputs video data in 4:2:2 format, multiplexed to 8-bit data words in Cb, Y, Cr, Y format. The UTIR-601 uses input signals field (B/T#) and horizontal sync (HSYNC#) to generate video timing. The STPC Video Controller can be configured to generate video timing (driving HSYNC# and B/T#) or lock to these signals when generated by an external video timing source. The OSD (On Screen Display) signal is not supported.

14.3.3. VIDEO PASS-THROUGH MODE

Note: VIP 1.0 video may not be compatible with passthrough mode if the video encoder depends on the SAV and EAV signals for video timing.

Video data can be accumulated in the Frame Buffer or simply passed through the Video Controller to a video encoder. Since there is no buffering in this mode, all components (in the video path) must be run at the same clock speed. In addition, the External Chip and the video encoder must be genlocked.

The incoming video stream and control signals are not decoded in any way; they are simply passed directly to the TV Output port as a constant, uninterrupted stream. Since there is no knowledge of video timing, the decimator must be disabled while using this mode, as it would corrupt the incoming data stream. Any ITU-R-656 extensions (SAV, EAV, ancillary data) present in the video stream are passed to the output unchanged.

This mode is included to allow raw video timing and data to be sent to the TV Output Port. The video port is disabled when pass through mode is selected. The timing of the B/T# and HSYNC# signals reflects the timing seen by an external device.

14.4. VIP SPECIFICATIONS NOT SUPPORTED

14.4.1. ANCILLARY DATA

The Video Input Port does not support the capture of Ancillary Data. The VIP specification allows this method to be used for capturing sliced VBI and digital audio PCM data through the Video Input Port.

Sliced VBI data cannot be transferred as ancillary data. It is intended that sliced VBI data be transferred from VIP compliant devices using the Host Port since only this method is available during MPEG playback.

Digital Audio PCM data cannot be transferred to the Frame Buffer. The specification for audio data transfer as Ancillary Data is still being developed by an ITU task force.

14.4.2. DMA CHANNEL RESTRICTIONS

The DMA controllers are only capable of accessing Host FIFO Space. They are not capable of accessing Host Register Space.

14.4.3. CHROMA MASK

There is no support provided for chroma key mixing since the STPC CRTC supports both colour and chroma based video mixing.

14.5. VIDEO INPUT MODULE ADDRESS SPACE

VIP Target devices are memory mapped into Graphics Register Space in the 4 Mbyte section allocated to memory mapped graphics and video registers. 256 Kbytes of this space are allocated to the Video Input Module. VIP Host Target Address Space occupies 32 Kbytes of this region. Host Port and DMA registers occupy another 32 Kbytes of this region. The Video Input Module Address Map is shown in [Table 14-2](#).

Table 14-2. Video Input Module Address Map

AD[31:28]	[27:24]	[23:20]	[19:18]	[17:15]	Description
0000	GBASE	0110	00	100	Video Input Port Registers - PIXCLK domain

VIDEO INPUT PORT

14.6. VIP VIDEO INPUT PORT REGISTERS

The video input port registers are all initialised to 0 at power up. Writes to registers marked reserved are ignored, reads always return 0.

14.6.1. FRAME BUFFER ADDRESS READBACK

The Frame Buffer address register is loaded from Vid_Ad0 or Vid_Ad1. A read path is provided at this address for testing purposes. The value is unsynchronised and should not be read during active video.

<i>FB1_Adr</i>										Access = 8400000h					Regoffset = 0x00h				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Rsv										FBA									
Default value after reset = 00000000h																			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
FBA																			
Default value after reset = 00000000h																			

Bit Number	Mnemonic	Description
Bits 31-22	Rsv	Reserved. This Read-Only field is reserved. When read it returns '0's.
Bits 21-0	FBA	Frame Buffer Address. Read-only static readback for Frame Buffer address register (for test). Lower address bits 2-0 are reserved and when read return a value of '0'.

14.6.2. VIDEO INPUT PORT CONFIGURATION REGISTER

The top byte of Vin_CFG is reserved for enabling and disabling interrupts. Bits 31-28 are used to reset interrupt enables. Individual interrupts are disabled by writing a '1' to the associated Reset IRQ enable field. Writing a zero to the Reset IRQ enable field preserves the existing enable status. Read values for these fields are undefined and should be masked off before comparing.

Bits 27 to 24 are the interrupt enables. Individual interrupts are enabled by writing a '1' to the associated interrupt enable field. Writing a zero preserves the existing value.

Writing a '1' to both the enable and reset enable field at the same time produces undefined results.

Vin_CFG

Access = 8400000h

Regoffset = 0x04h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rst_B FIEn	Rst_FI En	Rst_V BIEn	Rst_B OEn	BF_IE n	F_IEn	VB_IE n	BO_I En.	VCLK		ST	DE	AU	VIF		
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALEN	BS	FB1		FDC		FCC			DBE		EVC	FB1			IPE
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bit 31	Rst_BFIEn	Reset Buffer Full IRQ Enable (Write-only) 0: Preserve Buffer Full IRQ enable 1: Reset Buffer Full IRQ enable
Bit 30	Rst_FIEn	Reset Field IRQ Enable (Write-only) 0: Preserve Field IRQ enable 1: Reset Field IRQ enable
Bit 29	Rst_VBIEn	Reset Vertical Blank IRQ Enable (Write-only) 0: Preserve Vertical Blank IRQ enable 1: Reset Vertical Blank IRQ enable
Bit 28	Rst_BOEn	Reset Buffer Overflow IRQ Enable (Write-only) 0: Preserve Buffer Overflow IRQ enable 1: Reset Buffer Overflow IRQ enable
Bit 27	BF_IEEn	Buffer Full IRQ Enable 0: Preserve existing BF_IEEn value 1: IRQ is generated when either video input buffer goes full
Bit 26	F_IEEn	Field Change IRQ Enable 0: Preserve existing F_IEEn value 1: IRQ is generated when the internal Field bit changes
Bit 25	VB_IEEn	Vertical Blank IRQ Enable 0: Preserve existing VB_IEEn value 1: IRQ is generated at the end of the current field after flushing the frame buffer FIFO

VIDEO INPUT PORT

Bit Number	Mnemonic	Description
Bit 24	BO_IEn.	Video Input Buffer Overflow Enable 0: Preserve existing BO_IEn value 1: IRQ is generated when either video input buffer overflows (see vin_stat bit 24)
Bits 23-22	VCLK	VCLK source (see Table 14-3) VCLK source determines the clock source for the Video Input Port. A clock is required for the Video Input Port to respond to host accesses. The power on default is MCLK. VCLK is only an output when DCLK is the enabled source and the video port clock and timing signals are being generated by the CRTC. The following sequence is recommended when enabling the external VCLK. 1. Set vin_cfg[23:22] to '00' (Select MCLK for the internal timing). This insures that the VCLK pin is not being driven by the Video controller. 2. Enable the external VCLK driver. 3. Set vin_cfg[23:22] to '01' (Select VCLK for internal timing). This resets the time-out counter and selects the VCLK input. If the time-out counter (~16 MCLK periods) expires without detecting a valid VCLK input, the clock source will be changed back to MCLK. 4. Check vin_stat[9] to make sure that VCLK is present. Note: If video is not being captured correctly, vin_stat[9] should be checked to be sure that a valid VCLK is being provided.
Bit 21	ST	Start Buffer, Start_BF. Controls which video input buffer will be filled first. 0: Video input buffer 0 filled first 1: Video input buffer 1 filled first
Bit 20	DE	Decimator Enable, Dec_En. 0: No decimation of input pixels 1: Enable 2:1 video decimator
Bit 19	AU	Auto Update Auto_Up. This bit enables automatic updating of the displayed video buffer. 0: Buffer must be updated by the driver. 1: Buffer automatically switched to the most recently completed display buffer.
Bits 18-16	VIF	Video Input Format, VI_Form. This field controls how the video stream will be decoded. (See Table 14-4) In VIP 1.0 Video Mode the timing information is recovered from SAV and EAV codes embedded in the video stream. The video timing generator may be used to generate system timing In multiplexed CCIR-601 mode, the video input port can generate video timing or lock to an external source. Video timing generation is enabled for formats 0-3 and disabled for modes 4-7.
Bit 15: STPCC4 Version Only:	Rsv	Reserved. This Read-Only bit is reserved. When read it returns undefined data.
Bit 15: STPCC5 Version Only:	ALEN	Address Limit Enable: 0: Disable 1: Address Limitation Enable Enabled to prevent corrupt input video data overwriting memory. Makes use of limit address registers LADDR0 and LADDR1.

Bit Number	Mnemonic	Description
Bit 14	BS	Byte Swap. 0: Bytes within words are swapped on input to match the format expected by the video display, Y Cb Y Cr (default setting) 1: Bytes within words are passed directly through the input port. This setting should be selected in pass through mode to maintain Cb Y Cr Y format.
Bits 13-12	FB1	FB1 High Water Mark. HIGH ORDER 2 BITS of the Frame Buffer FIFO high water mark. Vin_cfg[13-12] and vin_cfg[3-1] are concatenated to form the video Frame Buffer FIFO high water mark. Video data is buffered between the video input port and the Frame Buffer in a FIFO (FB1). FB1 High Water Mark is used to optimise Frame Buffer accesses by specifying the point where FB1 makes a request to the Frame Buffer memory controller. When the Frame Buffer FIFO contains this number of QWORDS it will request access to the Frame Buffer.
Bits 11-10	FDC	Frame Drop Control. Frame Drop Control determines how often frames are captured. A Frame period consists of an odd and even field sequence, even when only one of the fields is captured. Frame dropping can be used to reduce the input video stream bandwidth when bottlenecks prevent capture and/or transmission at full video rates. (See Table 14-5)
Bits 9-7	FCC	Field Capture Control. Field Capture Control determines what fields are used to generate a frame. In progressive scan mode, fields are de-interlaced by merging odd and even fields into a single video buffer. This method of de-interlacing provides the highest vertical resolution but can cause motion artifacts where there are areas of movement. When capturing interlaced video in double buffer mode, the buffer is switched at the end of each enabled field (see Table 14-6)
Bit 6	DBE	Double Buffer Enable. Double Buffer Enable allows the amount of Frame Buffer memory to be reduced when capturing at less than full video rates. When single buffering is selected, all captured fields are written to the Frame Buffer using the buffer selected by the start buffer field 0: Single buffer 1: Double buffer
Bit 4	EVC	Enable Video Capture. Enable Video Capture starts or stops video capture operation. Video capture starts at the first enabled field of the next frame when video is being captured based on the field bit. When both fields are enabled, frame capture starts with field 1 (the odd field) as defined by ITU-R 656 . 0: Video capture will end after current frame 1: Video capture will begin at start of next frame or task
Bits 3-1	FB1	FB1 High Water Mark. LOW ORDER 3 BITS of the Frame Buffer FIFO high water mark.. See vin_cfg[13:12] for the high order bits.
Bit 0	IPE	Input Port Enable. The Input Port Enable allows the port to be reset by software. This bit should not be asserted during normal operation as it unconditionally resets the port to the default values . 0: Video input port disabled, counters/state machines initialised, capture of video stopped. 1: Video input port enabled

VIDEO INPUT PORT

Table 14-3. VCLK Source

Bit 23	Bit 22	VCLK source
0	1	Use MCLK for video timing generator and interface clock (default).
0	1	Use input VCLK for video interface clock.
1	0	Use DCLK for video interface clock.
1	1	Reserved

Table 14-4. Video Input Format

Bit 18	Bit 17	Bits 16	Video Input Format
0	0	0	VIP 1.0 Video Mode
0	0	1	Reserved
0	1	0	Pass through
0	1	1	STi3520A Compatibility mode (Multiplexed CCIR-601)
1	x	x	Reserved

Table 14-5. Frame Capture/Drop

Bit 11	Bits 10	Frame Capture/Drop
0	0	Capture all frames
0	1	Capture first frame, drop one, repeat
1	0	Capture first frame, drop two, repeat
1	1	Capture first frame, drop three, repeat

Table 14-6. Field Capture Control

Bit 9	Bit 8	Bits 7	Field Capture Control
0	0	0	Reserved
0	0	1	Interlaced mode, capture only odd fields
0	1	0	Interlaced mode, capture only even fields
0	1	1	Interlaced mode, capture both even and odd fields

14.6.3. VIDEO INPUT PORT STATUS REGISTER

Status bits that are latched are cleared by writing to `vin_stat` with a bit pattern that contains a '1' in the locations that are being reset and '0' in the locations that are to be preserved. Read only bits are unaffected by write cycles. Reserved bits are undefined and must be masked off before making comparisons.

<i>vin_stat</i>															
Access = 8400000h															
Regoffset = 0x08h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv															
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv				Ch2Int	Ch1Int	VCLK	VB	CP	F IRQ	VB IRQ	OEF	AB	BO IRQ	BF	B O F
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-12	Rsv	Reserved. This Read-Only field is reserved. When read it returns undefined data.
Bit 11	Ch2Int	Channel 2 Interrupt Pending Copy, Ch2Int. This bit is a read-only copy of the interrupt request bit in the DMA channel status register. It is provided here for convenience. See the description under DMA operation for more information.
Bit 10	Ch1Int	Channel 1 Interrupt Pending Copy, Ch1Int. This bit is a read-only copy of the interrupt request bit in the DMA channel status register. It is provided here for convenience. See the description under DMA operation for more information.
Bit 9	VCLK	VCLK present. This read-only bit reflects the presence of the VCLK signal 0: VCLK is not present 1: VCLK is present
Bit 8	VB	Vblank. This read-only bit reflects the value of the internal vertical blank 0: Active video region 1: Vertical blanking region
Bit 7	CP	Capture in Progress. This read-only bit is set at the start of the first video frame after Enable Capture of Video is set. It is cleared at the end of the first frame after Enable Capture of Video is cleared. This bit is controlled by hardware.
Bit 6	F IRQ	Field IRQ. This bit is set and latched when the digital field bit changes and the Field IRQ enable bit (<code>vin_cfg</code>) is set to 1. It is cleared by writing a value of 1 to <code>vin_stat[6]</code> .
Bit 5	VB IRQ	VBlank IRQ. This bit is set and latched when the last line of enabled video has been written to the Frame Buffer and the vblank IRQ enable bit (<code>vin_cfg</code>) is set to '1'. It is cleared by writing a value of '1' to <code>vin_stat[5]</code> .

VIDEO INPUT PORT

Bit Number	Mnemonic	Description
Bit 4	OEF	Odd/Even Field. This is a read only bit that reflects the value of the internal field flag (as defined by ITU-R 656). This status bit is not affected by the B/T# inversion control 0: Field 1 (Top field) is currently being processed 1: Field 2 (Bottom field) is currently being processed
Bit 3	AB	Active Buffer. This is a read only bit that reflects the value of an internal flag. It indicates which video buffer is currently being filled.
Bit 2	BO IRQ	Buffer Overrun IRQ. This bit is set and latched when either of the buffers receives a write from the pixel packer and the corresponding buffer full flag is set, indicating that a buffer overrun has occurred. If the corresponding interrupt enable is asserted, an interrupt is generated. This bit is cleared by writing a value of '1' to vin_stat[2].
Bit 1	BF	Buffer 1 Full. This bit is set and latched when buffer 1 receives the last pixel of a captured frame. This condition can, if enabled, generate an IRQ. This bit is cleared by writing a value of '1' to vin_stat[1].
Bit 0	B 0 F	Buffer 0 Full. This bit is set and latched when buffer 0 receives the last pixel of a captured frame. This condition can, if enabled, generate an IRQ. This bit is cleared by writing a value of '1' to vin_stat[0].

14.6.4. VIDEO INPUT BUFFER ADDR 0

Lines of video always start at a quad word boundary in the Frame Buffer. When the display window size is not a multiple of eight, any remaining bytes in the last quad word will be unused (and undefined). The LS three bits of this register are hardwired to zero to force QWORD alignment.

vin_ad0

Access = 8400000h

Regoffset = 0x0Ch

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv										VBA 0					
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBA 0															
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-22	Rsv	Reserved. This Read-Only field is reserved. When read it returns '0's
Bits 21-0	VBA 0	Video Buffer Addr 0. Quad word Frame Buffer start address for video input buffer 0. Lower address bits 2-0 are reserved and when read return a value of '0'.

VIDEO INPUT PORT

14.6.5. VIDEO INPUT BUFFER ADDR 1

The Least Significant three bits of this register are hardwired to zero to force QWORD alignment

vin_ad1

Access = 8400000h

Regoffset = 0x10h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv										VBA 1					
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBA 1															
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-22	Rsv	Reserved. This Read-Only field is reserved. When read it returns '0's
Bits 21-0	VBA 1	Video Buffer Addr 1. Quad word Frame Buffer start address for video input buffer 1. Lower address bits 2-0 are reserved and when read return a value of '0'.

14.6.6. VIDEO INPUT DEST PITCH

When the Field Capture Control selects one of the interlaced modes, the destination pitch is set to the number of quad words required to hold a line of video data. When de-interlacing by merging odd and even fields is selected, the destination pitch should be set to twice the number of quad words required to hold a line of video data. The Least Significant three bits of this register are hardwired to zero to force QWORD alignment.

vin_dp

Access = 8400000h

Regoffset = 0x14h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv															
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv		DP													
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-14	Rsv	Reserved. This Read-Only field is reserved. When read it returns '0's.
Bits 13-0	DP	Destination Pitch. This register holds the number of bytes in the Frame Buffer the beginning of one video scan line to the next. Lower address bits 2-0 are reserved and when read return a value of '0'.

VIDEO INPUT PORT

14.6.7. EXTERNAL TIMING GENERATOR 1

vtg_ext1

Access = 8400000h

Regoffset = 0x28h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VGT	Rsv	Bt_oe	HSYN C_OE	Rsv	Bt_pol	HSYN C_PO L	Rsv	GM			Rsv			HS_St	
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS_St				Rsv			HS_End								HS_Cdd
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bit 31	VGT	VTG enable. 0: Video timing is reset to the start of field 1 1: Video timing generator is enabled
Bit 30	Rsv	Reserved. This Read-Only field is reserved. When read it returns undefined data.
Bit 29: STPCC4 Version Only:	Bt_oe	Output enable for the B/T# video timing signal , bt_oe. Set to '1' when the Video Controller is generating the system video timing signals. 0: B/T# is an input 1: B/T# is an output
Bit 29: STPCC5 Version Only:		VSYNC Signal direction, see Section 12.9.33. for detailed application
Bit 28: STPCC4 Version Only:	HSYNC_OE	Output enable for the HSYNC- video timing signal, hsync_oe. Set to '1' when the Video Controller is generating the system video timing signals. 0: HSYNC# is an input 1: HSYNC# is an output
Bit 28: STPCC5 Version Only:		HSYNC Signal direction, see Section 12.9.33. for detailed application
Bit 27	Rsv	Reserved. This Read-Only field is reserved. When read it returns undefined data.
Bit 26	Bt_pol	B/T# polarity, bt_pol. This bit defines the active edge for the B/T# signal as input and output. The setting of this bit sets the polarity of the external signal to be high or low true. The polarity of the internal field (F) and horizontal blank (H) bits are not affected. 0: B/T# is low for field 1 1: B/T# is high for field 1
Bit 25	HSYNC_POL	HSYNC# polarity, hsync_pol. This bit defines the active edge for the HSYNC# signal as input and output. The setting of this bit sets the polarity of the external signal to be high or low true. The polarity of the internal field (F) and horizontal blank (H) bits are not affected by these bits. 0: HSYNC# is low true 1: HSYNC# is high true

Bit Number	Mnemonic	Description
Bit 24	Rsv	Reserved. This Read-Only field is reserved. When read it returns undefined data.
Bits 23-21	GM	Genlock Mode. Defines the method for genlocking to an external source. (See Table 14-7).
Bits 20-18	Rsv	Reserved. This Read-Only field is reserved. When read it returns undefined data.
Bits 17-12	HS_St	Leading edge of HSYNC# in pixels, HS_St. Allows the HSYNC# trailing edge to be shifted relative to the start of the horizontal line in pixels, referenced to the horizontal counter. Since the video clock runs at twice the pixel rate, this value must be multiplied by 2 (shifted left 1) before being compared to the horizontal count. HS_Odd is used to generate the least significant bit, insuring that HSYNC# can be generated at any point during the horizontal scan line.
Bits 11-9	Rsv	Reserved. This Read-Only field is reserved. When read it returns undefined data.
Bits 8-1	HS_END	Trailing edge of HSYNC# in pixels, HS_End. Allows the HSYNC# trailing edge to be shifted relative to the end of a horizontal line in pixels, referenced to the horizontal counter. Since the video clock runs at twice the pixel rate, this value must be multiplied by 2 (shifted left 1) before being compared to the horizontal count. HS_Odd is used to generate the least significant bit, insuring that HSYNC# can be generated at any point during the horizontal scan line.
Bit 0	HS_ODD	HSYNC# Odd compensation, HS_Odd. This bit allows the leading and trailing edges of HSYNC# to be shifted by 1 VCLK to compensate for an odd number of pipe stages between the video input port and an external device. This bit is used as the least significant bit of HS_End and HS_St when being compared to the horizontal counter. When the video timing generator is in master mode, the leading edge of the external HSYNC occurs on the clock edge following when the horizontal counter matches the HSSt value. The trailing edge occurs on the clock edge following when the horizontal counter matches the HSEnd value. When the video timing generator is in slave mode, the horizontal counter is set to HSSt value on the second VCLK edge following HSYNC# assertion. In slave mode, the horizontal timing is independent of the trailing edge of HSYNC# and HSEnd is ignored. The default values are specified to match ITU-R 656 (525 line) timing in slave mode.

Table 14-7. Genlock Mode

Bit 23	Bit 22	Bit 21	Genlock Mode
0	0	0	No genlocking. Video timing generator resets horizontal and vertical counters based on H_Total and V_Total. (default)
0	0	1	Genlock to B/T# and HSYNC#
0	1	0	Genlock to SAV/EAV codes
		1xx	Reserved

VIDEO INPUT PORT

14.6.8. EXTERNAL TIMING GENERATOR 2

vtg_ext2

Access = 8400000H

Regoffset = 0x2Ch

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv											BT_Dly1				
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BT_Dly1					BT_Dly2										BT_Cdd
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-21	Rsv	Reserved. This Read-Only field is reserved. When read it returns '0's.
Bits 20-11	BT_Dly1	B/T# delay for field 1 in pixels, BT_Dly1. This field determines the location relative to the horizontal counter that B/T# switches to indicate field 2 of an interlaced frame.
Bits 10-1	BT_Dly2	B/T# delay for field 2 in pixels, BT_Dly2. This field determines the location relative to the horizontal counter that B/T# switches to indicate field 2 of an interlaced frame.
Bit 0	BT_Odd	B/T## Odd compensation, BT_Odd. This bit allows the leading and trailing edges of B/T# to be shifted by 1 VCLK to compensate for an odd number of pipe stages between the video input port and an external device. This bit is used as the least significant bit of BT_Dly1 and BT_Dly2 when being compared to the horizontal counter.

14.6.9. HORIZONTAL TIMING GENERATOR

vtg_ht

Access = 8400000H

Regoffset = 0x30h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
H_Start										Rsv	H_End					
Default value after reset = 00000000h																

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H_End					Rsv	H_Total									
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-22	H_Start	Horizontal start of active video in pixels, H_Start. When video capture is based on the video timing generator, The H_Start and H_End values are used to determine when video is captured within the vertical display window.
Bit 21	Rsv	Reserved. This Read-Only field is reserved. When read it returns undefined data.
Bits 20-11	H_End	Horizontal end of active video in pixels, H_End.
Bit 10	Rsv	Reserved. This Read-Only field is reserved. When read it returns undefined data.
Bits 9-0	H_Total	Total number of horizontal pixels, H_Total. This field contains the total number of pixels per line.

VIDEO INPUT PORT

14.6.10. VIDEO TIMING GENERATOR

V_Start specifies the first line of active video in each field.

V_End specifies the last line of active video in each field.

vtg_vt

Access = 8400000h

Regoffset = 0x34h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V_Start										Rsv	V_End				
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V_End					Rsv	V_Total									
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-22	V_Start	Vertical Field Start, V_Start. Line number of the last line of blanked video in each field. The first line of active video is V_Start + 1
Bit 21	Rsv	Reserved. This Read-Only field is reserved. When read it returns undefined data.
Bits 20-11	V_End	Vertical Field End, V_End. Line number of the last line of active video in each field.
Bit 10	Rsv	Reserved. This Read-Only field is reserved. When read it returns undefined data.
Bits 9-0	V_Total	Vertical Total, V_Total. V_Total contains the total number of lines in a field. When the internal vertical counter reaches the value contained in V_Total it restarts from either count zero or count one, depending on the field. It gets reset to 1 at the beginning of field 1, making the number of lines in field 1 equal to V_Total. At the beginning of field 2 it gets reset to zero making the number of lines V_Total + 1. The internal field bit (F) gets inverted coincident with the resetting of the vertical and horizontal counters.

14.6.11. LIMIT ADDRESS REGISTERS (STPCC5 Version Only)

Fill the limit address registers of frame buffers 0 and 1.

Laddr0												Access = 8400000h			Regoffset = 0x3Ch		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Rsv												Laddr0[21:3]					
Default value after reset = 00000000h																	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Laddr0[21:3]															
Default value after reset = 00000000h															

<i>Laddr1</i>												Access = 8400000h			Regoffset = 0x38h		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Rsv												Laddr1[21:3]					
Default value after reset = 00000000h																	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Laddr1[21:3]															
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31:19	Rsv	Reserved. This Read-Only field is reserved. When read it returns undefined data.
Bits 18:0	Laddr0/1	Limit Address Registers of Frame Buffers 0 and 1: When the current address is greater than the limit address, this address is then held at the same value until the end of capture of the given field is reached, i.e. until vertical blanking occurs. This function, enabled by bit 15 of the Video Input Port Configuration register, is used to prevent memory overrun. When not enabled, corrupted video input data can cause the VMI module to continue to write to memory by incrementing the address, thereby causing memory to be over-written.

15. VIDEO PIPELINE REGISTERS

15.1. INTRODUCTION

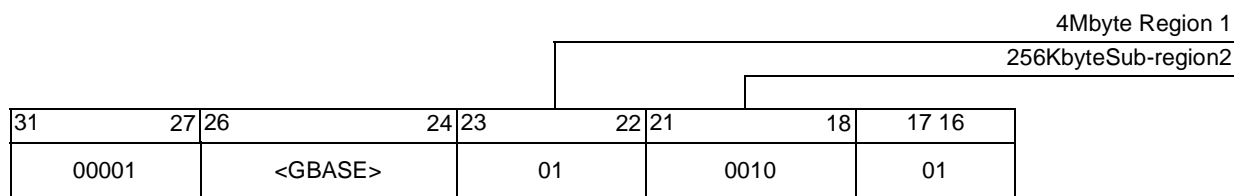
The STPC video input signals, buffering and TV output signals are managed by the Video Controller, where the video input and display signals are controlled through the Video Pipeline registers. These registers, which control the settings for the display buffer areas, plus filter control, colour mixing and colour space mixing, are described in the remainder of this Chapter.

The video input signal and buffering are controlled by the Video Input Port. This port interfaces with external digital video signals in various formats, and is described in the separate Video Input Port Chapter.

Finally, the TV Output Port, which controls the video TV output signal in various standard formats, is a high-performance PAL/NTSC TV digital encoder. This converts the digital video signal stream into a standard analog baseband PAL/NTSC TV signal, and also produces the RGB analog components. It supports both interlaced (525 line and 625 line standards) and non-interlaced modes. The supported signal encoding formats include NTSC-M, PAL-B, D, G, H, I, N, M, plus NTSC-4.43 encoding. It can also perform Closed-Caption or CGMS encoding. The TV Output Port is described in the separate TV Output Port Chapter.

15.2. VIDEO PIPELINE REGISTER LOCATIONS

The Video Pipeline registers, similar to the extended graphics (non-VGA) registers, are located in the 4-MByte memory-mapped registers region of the 16-MByte memory space occupied by the Graphics Controller. The Video Pipeline registers are located at the 256-KByte wide sub-region 2. The diagram below shows the address format for the Video Pipeline registers.



All registers can be read with accesses of any width. The CPU can read any register via byte (8-bit), word (16-bit), or double-word (32-bit) accesses. Writes must be done using double-word (32-bit) transfers.

VIDEO PIPELINE REGISTERS

15.3. SOURCE SPECIFICATION REGISTERS

15.3.1. VIDEO_SRC_BASE

This register specifies the DRAM linear starting address of the source image, aligned to an eight byte boundary. This address may specify either the top left corner or bottom left corner, depending on the state of the Y_Vid_Src_dir bit in the Video_Src_Pitch register.

This register is double buffered; the active register is only updated during vertical blanking.

Video_Src_Base

Access = X480000h

Regoffset = 000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv										VSI					
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSI															
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-22	Rsv	Reserved.
Bits 21-0	VSI	Base linear address of the Video Source Image. Lower address bits 2-0 are reserved and when read return a value of '0'.

15.3.2. VIDEO_SRC_PITCH

This register contains the Video_Src_pitch field. This specifies the number of bytes which must be added to the address of a pixel on one line of the video source image to compute the address of the corresponding pixel on the line below.

This register also contains the Y_Vid_Src_dir bit, which specifies the Y direction in which the Video Source Image should be read, and the Video_Colour_fmt field which defines the the Colour format of the Video Source Image.

Video_Src_Pitch																Access = X480000h				Regoffset = 0x04h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16								
Rsv																							
Default value after reset = 00000000h																							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv		VSI		Y_V_S_D	Current_Ad										
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-14	Rsv	Reserved.
Bits 13-12	VSI	Video Source Image colour format: 00 - RGB 555 01 - RGB 565 10 - YUV 422
Bit 11	Y_V_S_D	Y_Vid_Src_dir. Specifies the Y direction in which the Video Source Image should be read. This bit controls the translation of XY addresses to linear DRAM addresses. If(Y_Vid_Src_dir == 0) DRAM linear address = Video_Src_Base + (YDIFF * Vid_Src_Pitch); Else DRAM linear address = Video_Src_Base - YDIFF * Vid_Src_Pitch); Where YDIFF is a 1 bit value that varies.
Bits 10-0	Current_Ad	Specifies the amount to add to the current address to get to the address of the corresponding pixel in the next line. Lower address bits 2-0 are reserved and when read return a value of '0'.

Programming Notes:

This register also contains the Y_Vid_Src_dir bit which specifies the Y direction in which the Video Source Image should be read, and the Video_Colour_fmt field which defines the the Colour format of the Video Source Image.

VIDEO PIPELINE REGISTERS

15.3.3. VID_SRC_DIM

This register contains the dimensions of the Video Source Image relative the the starting corner.

This register is double buffered. The active register is only updated during vertical sync.

Vid_Src_dim

Access = X480000h

Regoffset = 0x08h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv						dY									
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv						dX									
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-26	Rsv	Reserved.
Bits 25-16	dY	dY , the height of the Video Source image - 1, in lines, from the starting corner to the end of the image (dependent on Y_Vid_Src_dir)
Bits 15-10	Rsv	Reserved.
Bits 9-0	dX	dX , the width in pixels, of a line

This register is double buffered. The active register is only updated during vertical sync.

15.3.4. CRTC_BURST_LENGTH

This register contains the CRTC low water mark and burst length.

CRTC_Burst_length

Access = X480000h

Regoffset = 0x0Ch

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Crtc_Dlwm								Crtc_lwm							
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Crtc_dt					Rsv	Crtc_Bl									
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-24	Crtc_Dlwm	<p>Delta low water mark, crtc_dlwm. Together with crtc_dt and crtc_lwm, this field defines a variable low water mark. When the video window starts, the CRTC low water mark is set to crtc_lwm. After that time, for every crtc_dt*8 pixels' time elapsed, the low water mark will be incremented by crtc_dlwm bytes.</p> <p>Since this field is represented as a 2's complement number, setting bit 31 results in a low water mark which is a decreasing function of time. A decreasing or constant function will be the normal mode of operation of the CRTC low water mark during the video window.</p> <p>Note that this CRTC low water mark is distinct from the one described in CR1B. This one is valid during the video windows only.</p> <p>For normal CRTC operation (scanlines or pixels outside the video window), the pertinent CRTC low water mark is specified by CR1B.</p> <p>Guarantee of the CRTC ownership can be achieved by the Setting of this field to zero. This causes the CRTC low water mark to remain at a constant value of crtc_lwm.</p>
Bits 23-16	Crtc_lwm	<p>crtc_lwm, the (initial) low water mark for the CRTC FIFO in bytes. During the video window, if the CRTC FIFO occupancy rises above the low water mark (defined as a function of time by crtc_dlwm and crtc_dt) and the video occupancy rises above the video low water mark then ownership of the system DRAM can be given back to the CPU.</p> <p>The value of this register field can only be a multiple of eight (bits 18-16 are not writable and read as zeroes).</p>
Bits 15-11	Crtc_dt	crtc_dt, delta t. See the description of crtc_dlwm above.
Bit 10	Rsv	Reserved.
Bits 9-0	Crtc_Bl	<p>Minimum CRTC burst length, crtc_bl. This is the minimum number of bytes that will be sent in one transfer to fill the CRTC FIFO (during the active video window only). This value can only be a multiple of eight (bits 2-0 are not writable and read as zeroes) since pixels are fetched 8 bytes at a time.</p>

VIDEO PIPELINE REGISTERS

15.3.5. VID_BURST_LENGTH

This register is the video counterpart of the previous register. It specifies the video low water mark and burst length.

Vid_Burst_length

Access = X480000h

Regoffset = 0x10h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Vid_Dlwm								Vid_lwm							
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vid_Dt					Rsv	Vid_Bl									
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-24	Vid_Dlwm	Delta low water mark, vid_dlwm. Together with vid_dt and vid_lwm, this field defines a variable low water mark. When the video window starts, the video low water mark is set to vid_lwm. After that time, for every vid_dt*8 pixels' time elapsed, the low water mark will be incremented by vid_dlwm bytes. As with crtc_dlwm, above, This field is a 2's complement number. Setting this field to zero causes the video low water mark to remain at a constant value of vid_lwm.
Bits 23-16	Vid_lwm	vid_lwm , the (initial) low water mark for the video FIFO in bytes. During the video window, if the video FIFO occupancy rises above the low water mark (defined as a function of time by vid_dlwm and vid_dt) and the crtc occupancy rises above crtc_lwm then ownership of the system DRAM can be given back to the CPU. The value of this register field can only be a multiple of eight (bits 18-16 are not writable and read as zeroes).
Bits 15-11	Vid_Dt	vid_dt, delta t. See the description of vid_dlwm above.
Bit 10	Rsv	Reserved.
Bits 9-0	Vid_Bl	Minimum video burst length, vid_bl. This is the minimum number of bytes that will be sent in one transfer to fill the video FIFO. This value can only be a multiple of eight (bits 2-0 are not writable and read as zeroes) since pixels are fetched 8 bytes at a time.

15.4. DESTINATION SPECIFICATION REGISTERS

15.4.1. VID_DST_XY

This register contains the coordinates of the top left corner of the video window.

This register is double buffered. The active register is only updated during vertical sync.

Vid_Dst_XY						Access = X480000h						Regoffset = 0x14h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv						Y									
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv					X										
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-26	Rsv	Reserved.
Bits 25-16	Y	Y, the Y coordinate of the top edge of the video window, relative to the display. The first display line is line 0.
Bits 15-11	Rsv	Reserved.
Bits 10-0	X	X, the X coordinate of the left edge of the video window, relative to the display. The first pixel of each display line is pixel 0.

Programming Notes:

This register is double buffered. The active register is only updated during vertical sync.

VIDEO PIPELINE REGISTERS

15.4.2. VID_DST_DIM

This register contains the dimensions of the video window.

This register is double buffered. The active register is only updated during vertical sync.

Vid_Dst_dim

Access = X480000h

Regoffset = 0x18h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv						dY									
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv					dX										
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-26	Rsv	Reserved.
Bits 25-16	dY	dY , the height of the video window in screen lines - 1 is entered in this field.
Bits 15-11	Rsv	Reserved.
Bits 10-0	dX	dX , the width of the video window in screen pixels.

Programming Notes:

This register is double buffered. The active register is only updated during vertical sync.

15.5. FILTER CONTROL REGISTERS**15.5.1. HORIZ_SCALE**

This register contains the control for horizontal scaling and decimation.

This register is double buffered. The active register is only updated during vertical sync.

Horiz_Scale										Access = X480000h				Regoffset = 0x20h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Rsv											F0E	F1E	Rsv				
Default value after reset = 00000000h																	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv			HPI												
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-21	Rsv	Reserved.
Bit 20	F0E	Filter Enable 0, F0E. When in YUV modes, this bit enables the interpolator for the Y channel, and in RGB modes enables all three interpolators. If this bit is 0, pixel replication is used.
Bit 19	F1E	Filter Enable 1, F1E. When in YUV modes, this bit enables the interpolators for the U and V channels. If this bit is 0, pixel replication is used. This bit controls the RGB components in RGB modes and should be the same as F0E.
Bits 28-16	Rsv	Reserved.
Bits 15-13	Rsv	Reserved.
Bits 10-0	HPI	Horizontal Phase Increment, hpi. Defines the horizontal scale factor. hpi is calculated from source width and destination width:- $\text{hpi} = ((\text{source_width}/\text{hdf_tmp}) * 4096)/\text{dest_width}$ Note that the maximum value hpi is 4096.

Programming Notes:

This register is double buffered. The active register is only updated during vertical sync.

VIDEO PIPELINE REGISTERS

15.5.2. VERT_SCALE

This register contains the control for vertical scaling and decimation.

This register is double buffered. The active register is only updated during vertical sync.

Vert_Scale											Access = X480000h		Regoffset = 0x28h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Rsv											VF0E	VF1E	Rsv			
Default value after reset = 00000000h																

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv			VPI												
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-21	Rsv	Reserved.
Bit 20	VF0E	Vertical Filter Enable 0, VF0E. When in YUV modes, this bit enables the interpolator for the Y channel, and in RGB modes enables all three interpolators. If this bit is 0, pixel replication is used.
Bit 19	VF1E	Vertical Filter Enable 1, VF1E. When in YUV modes, this bit enables the interpolators for the U and V channels. If this bit is 0, pixel replication is used. This bit controls the RGB components in RGB modes and should be the same as VF0E.
Bits 28-16	Rsv	Reserved.
Bits 15-13	Rsv	Reserved.
Bits 12-0	VPI	Vertical Phase Increment, vpi. Defines the vertical scale factor. vpi is calculated from source height and destination height:- $vpi = (source_height * 4096) / dest_height$ Note that the maximum value for vpi is 4096

Programming Notes:

This register is double buffered. The active register is only updated during vertical sync.

15.5.3. COLOUR SPACE CONVERTER SPECIFICATION

This register contains the control for the Colour Space Converter.

Colour space converter specification

Access = X480000h

Regoffset = 0x2Ch

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv															
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv															CSCE
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-1	Rsv	Reserved.
Bit 0	CSCE	Colour Space Converter Enable. When set, YUV data is converted to RGB according to the formula:- $R = 1.164(Y - 16) + 1.591(V - 128)$ $G = 1.164(Y - 16) - 0.700(V - 128) - 0.336(U - 128)$ $B = 1.164(Y - 16) + 1.733(U - 128)$ When clear, pixels are passed through unchanged.

Programming Notes:

VIDEO PIPELINE REGISTERS

15.6. VIDEO AND GRAPHICS MIXING CONTROL REGISTERS

15.6.1. MIX MODE REGISTER

This register contains the Mix_Mode field which defines the method used to mix graphics and video.

<i>Mix_Mode</i>															
Access = X480000h															
Regoffset = 0x30h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv															
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv														MM	
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-2	Rsv	Reserved.
Bits 1-0	MM	Mix_Mode , controls the way in which graphics and video are mixed. (See Table 15-1)

Table 15-1. Mix Mode

1	0	Mix Mode
0	0	Video Window only. The video always appears in a rectangular window which is defined by the Destination Specification registers.
0	1	Video Window with Colour Key. The Destination specification is further qualified by the Colour Key register. Within the specified video window, if the graphics pixel (pre colour palette) is equal to the value specified by the Colour Key register, then the corresponding video pixel is displayed, otherwise the graphics pixel is displayed. Note that in 8-bit graphics modes, only Colour_Key[7:0] are used in the comparison and in 16-bit graphics modes, Colour_Key[15:0] are used.
1	0	Video Window with Chroma Key. The destination specification is qualified by the Chroma key registers. Chroma key compares each of the pixel components to independent 'high' and 'low' values (between limits compare). If all the selected components are between their limits, then the corresponding graphics pixel is displayed, otherwise the video pixel is displayed. Note that the video pixel can be compared either before or after the Colour Space Converter. Note also that the chrom key can be programmed to ignore any or all component values.
1	1	Reserved

15.6.2. COLOUR KEY REGISTER

This register contains the colour key value used in colour keying mixing.

CCLR_Key

Access = X480000h

Regoffset = 0x34h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv								CK							
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CK															
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-2	Rsv	Reserved.
Bits 1-0	CK	Colour_Key , this value is compared to the graphics pixel to determine whether to display the video pixel in colour key mode. When the graphics is operating in 8-bit per pixel mode, Colour_key[7:0] is compared, when the graphics is operating in 16-bits per pixel, Colour_Key[15:0] is compared and when the graphics is operating in 24-bits per pixel, Colour_Key[23:0] is compared.

VIDEO PIPELINE REGISTERS

15.6.3. CHROMA KEY LOW REGISTER

This register contains the chroma key low limits, the component ignore bits and the colour mode bit used in chroma keying mixing.

CKL

Access = X480000h

Regoffset = 0x38h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv				CK	IC2	IC1	IC0	CH2L							
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH1L								CH0L							
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-28	Rsv	Reserved.
Bit 27	CK	Chroma key mode. 0: Components examined at input to colour space converter (YUV mode) 1: Components examined at output of colour space converter (RGB mode)
Bit 26	IC2	Ignore component 2. If set, component 2 (V or B) is ignored in the chroma key comparison.
Bit 25	IC1	Ignore component 1. If set, component 1 (U or G) is ignored in the chroma key comparison.
Bit 24	IC0	Ignore component 0. If set, component 0 (Y or R) is ignored in the chroma key comparison.
Bits 23-16	CH2L	ch2low , the low limit against which component 2 is compared during chroma key operations.
Bits 15-8	CH1L	ch1low , the low limit against which component 1 is compared during chroma key operations.
Bits 7-0	CH0L	ch0low , the low limit against which component 0 is compared during chroma key operations.

15.6.4. CHROMA KEY HIGH REGISTER

This register contains the chroma key high limits used in chroma keying mixing.

CKH								Access = X480000h				Regoffset = 0x3Ch			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rsv								CH2H							
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH1H								CH0H							
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bits 31-24	Rsv	Reserved.
Bits 23-16	CH2H	ch2high , the high limit against which component 2 is compared during chroma key operations.
Bits 15-8	CH1H	ch1high , the high limit against which component 1 is compared during chroma key operations.
Bits 7-0	CH0H	ch0high , the high limit against which component 0 is compared during chroma key operations.

The operation of the chroma key can be summarised as follows:-

```

Let Cn represent component n, n = 0..2
Let Chnlow represent Chlow for component n, n = 0..2
Let Chnhigh represent Chigh for component n, n = 0..2
Kn be the result of the compare for component n, n = 0..2
for(n = 0; n < 3; n++)
  if((Cn >= Chnlow) && (Cn <= chmhigh))
    Kn = 1
  else
    Kn = 0
If((I0||K0) && (I1||K1) && (I2||K2))
  display graphics pixel
else
  display video pixel
  
```

VIDEO PIPELINE REGISTERS

15.6.5. STATUS REGISTER

This register contains enable bit for the video scaler.

Filter_Stat

Access = X480000h

Regoffset = 0x40h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V_En	Rsv														
Default value after reset = 00000000h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsv															
Default value after reset = 00000000h															

Bit Number	Mnemonic	Description
Bit 31	V_En	vid_enable. Setting the enable bit turns on the video scaler.
Bits 30-0	Rsv	Reserved.

16. TV OUTPUT PORT

16.1. INTRODUCTION

The STPC video input signals, buffering and TV output signals are managed by the Video Controller. The TV Output Port, which controls the video TV output signal in various standard formats, is a high-performance PAL/NTSC TV digital encoder. This converts the digital video signal stream into a standard analog baseband PAL/NTSC TV signal, and also produces the RGB analog components. It supports both interlaced (525 and 625 line standards) and non-interlaced modes. The supported signal encoding formats include NTSC-M, PAL-B, D, G, H, I, N, M, plus NTSC-4.43 encoding. It can also perform Closed-Caption or CGMS encoding. The TV Output Port is described in the remainder of this Chapter.

The video input signal and buffering are controlled by the Video Input Port. This port interfaces with external digital video signals in various formats, and is described in the separate Video Input Port Chapter.

Finally, the video input and display signals are controlled through the Video Pipeline registers. These registers, which control the settings for the display buffer areas, plus filter control, colour mixing and colour space mixing, are described in the separate Video Pipeline Register Chapter.

16.2. FUNCTIONAL DESCRIPTION

The TV Output Port can operate either in master mode, where it supplies all sync signals, or in six slave modes, where it locks onto incoming sync signals.

16.2.1. DATA INPUT FORMAT

The digital input signal from the Video Input Port (in Passthrough mode), or the regenerated video input signal, is expected to appear as a time-multiplexed, ITU-R656 /D1-type [Cb, Y, Cr, Y], 8-bit stream.

Note: "ITU-R" was formerly known as "CCIR".

Input samples are latched on the rising edge (by default) of the clock signal CKREF, whose nominal frequency is 27 MHz. Figure 1 illustrates the expected data input format. Alternatively, a 54-Mbit/s stream can be fed to the TV Output Port. Refer to the STV0119A PAL/NTSC High Performance Digital Encoder Data Sheet, Section IV.17, Dual Encoding Application 54 Mbit/s YCrCb Interface, for further details.

The TV Output Port is able to encode interlaced and non-interlaced video. One bit is sufficient to automatically direct the TV Output Port to process non-interlaced video. Update is performed internally on the first frame sync active edge following the programming of this bit. The non-interlaced mode is a 624 divided-by-two line mode (312 lines) or a 524 divided-by-two line mode (262 lines), where all fields are identical.

An 'autotest' mode is available by setting three bits (sync[2:0]) within Configuration Register_0. In this mode, a colour bar pattern is produced, independently from video input, in the appropriate standard.

As this mode sets the TV Output Port in master mode, VSYNC/ODDEV and HSYNC pins are then in output mode.

16.2.2. VIDEO TIMING

The TV Output Port outputs interlaced or non-interlaced video in PAL-B, D, G, H, I, PAL-N, PAL-M or NTSC-M standards and 'NTSC-4.43' is also possible.

The four-frame (for PAL) or two-frame (for NTSC) burst sequences are internally generated, subcarrier generation being performed numerically with CKREF as reference. Rise and fall times of synchronization tips and burst envelope are internally controlled according to the relevant ITU-R and SMPTE recommendations.

TV OUTPUT PORT

It is possible to allow encoding of incoming YCrCb data on those lines of the VBI that do not bear line sync pulses or pre/post-equalisation pulses. This mode of operation is referred to as "partial blanking" and is the default setup. It allows the retention in the encoded waveform of any VBI data present in digitised form in the incoming YCrCb stream (e.g. WSS data, VPS, supplementary Closed-Captions line, StarSight data, etc.). Alternatively, the complete VBI may be blanked (no incoming YCrCb data encoded on these lines, "full blanking").

The complete VBI comprises the following lines:

For 525/60 systems (SMPTE line numbering convention): lines 1 to 19 and second half of line 263 to line 282.

For 625/50 systems (CCIR line numbering convention): second half of line 623 to line 22 and lines 311 to 335.

The 'partial' VBI consists of :

For 525/60 systems (SMPTE line numbering convention): lines 1 to 9 and second half of line 263 to line 272.

For 625/50 systems (CCIR line numbering convention): second half of line 623 to line 5 and lines 311 to 318.

Full or partial blanking is controlled by configuration bit 'blkli in configuration register1'.

Note that line 282 in 525/60/SMPTE systems is either fully blanked or fully active, line 23 in 625/60/CCIR systems is always fully active.

In an ITU-R656-compliant digital TV line, the active portion of the digital line is the portion included between the SAV (Start of Active Video) and EAV (End of Active Video) words. However, this digital active line starts somewhat earlier and may end slightly later than the active line usually defined by analog standards. The TV Output Port allows two approaches :

- 1) It is possible to encode the full digital line (720 pixels/1440 clock cycles). In this case, the output waveform will reflect the full YCrCb stream included between SAV and EAV.
- 2) Alternatively, it is possible to drop some YCrCb samples at the extremities of the digital line so that the encoded analog line fits within the 'analog' ITU-R/SMPTE specifications.

Selection between these two modes of operation is performed with bit 'aline' in configuration register 4.

In all cases, the transitions between horizontal blanking and active video are shaped to avoid too steep edges within the active video. [Figure 16-1](#) gives timings for the horizontal blanking interval and the active video interval.

16.2.3. RESET PROCEDURE

After a hardware reset, the TV Output Port is set in HSYNC+ODDEV (line-locked) slave mode, for NTSC-M, interlaced ITU-R601 encoding. Closed-captioning is disabled.

The configuration can be customised by writing into the appropriate registers. A few registers are never reset, their contents is unknown until the first loading (refer to the Register Contents and Description paragraphs).

It is also possible to perform a software reset by setting bit 'softreset' in Reg 6. The TV Output Port's response in this case is similar to the response after a hardware reset, except that Configuration Registers (Reg 0 to 6) and a few other registers (see description of bit 'softreset' in [Section 16.6.7.](#)) are not altered .

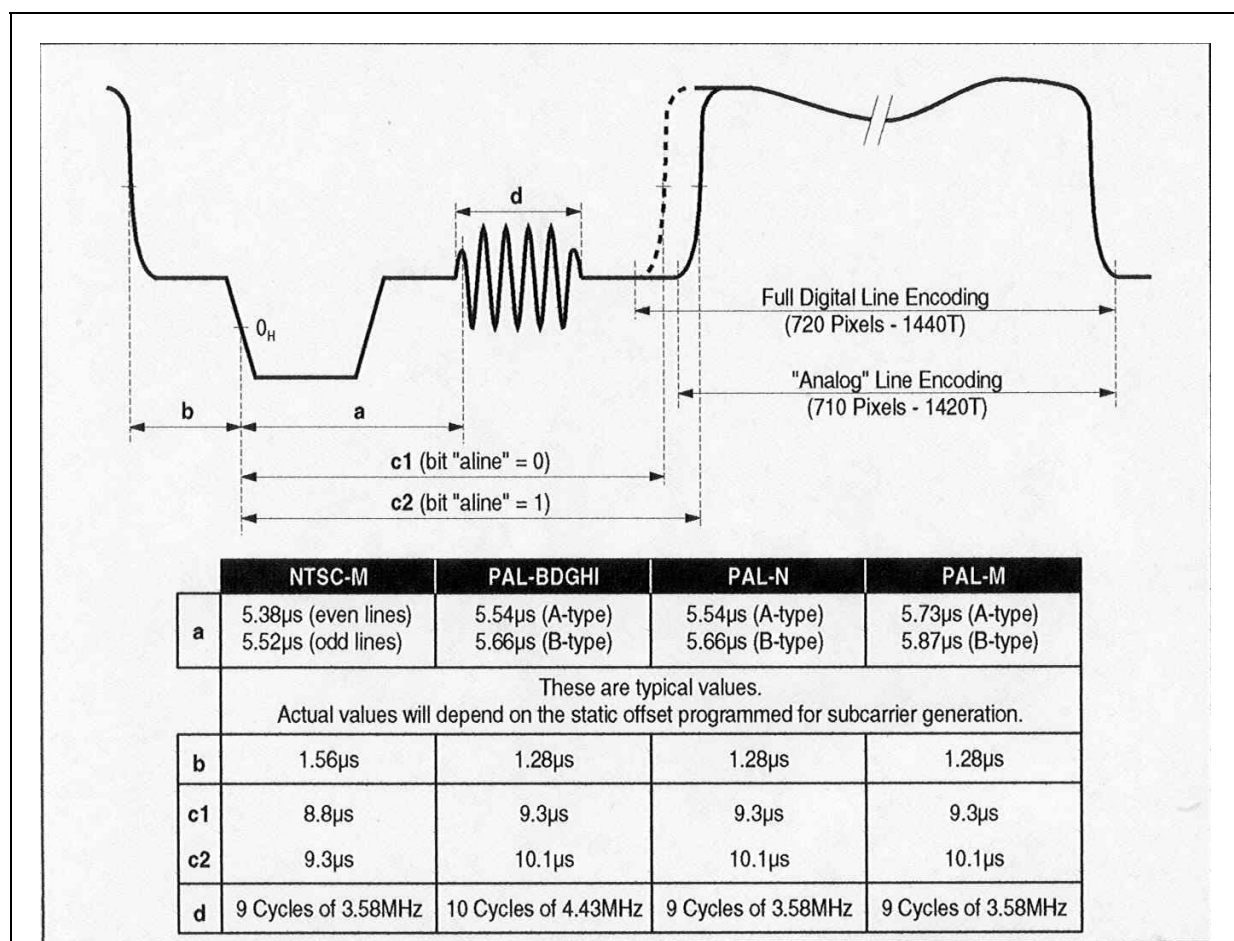


Figure 16-1. Horizontal Blanking Interval and Active Timings

16.2.4. MASTER MODE

In this mode, the TV Output Port supplies HSYNC and ODDEV sync signals (with independently programmable polarities) to drive other blocks. Refer to [Figure 16-2](#) and [Figure 16-3](#) for timings and waveforms.

The TV Output Port starts encoding and counting clock cycles as soon as the master mode has been loaded into the control register (Reg.0 - see [Section 16.6.1](#).)

Configuration bits "Syncout_ad[1:0]" (Reg.4 - see [Section 16.6.5](#).) allow for the shifting of the relative position of the sync signals by up to three clock cycles to cope with any YCrCb phasing

TV OUTPUT PORT

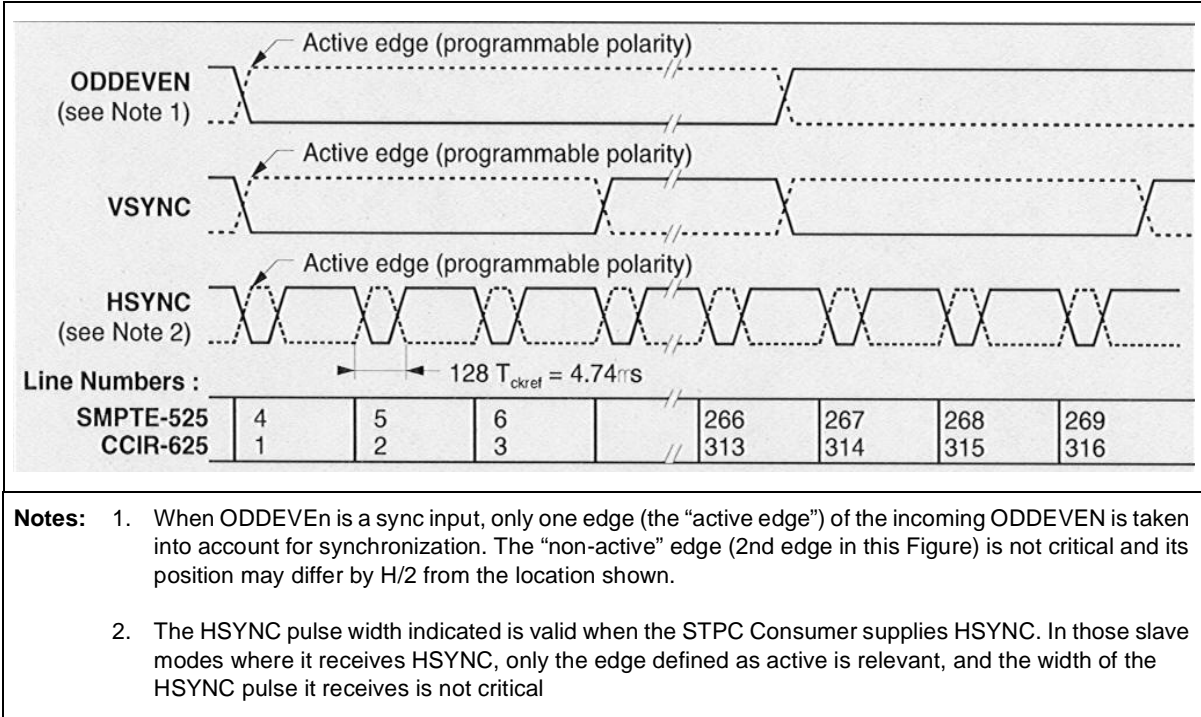


Figure 16-2. ODDEVEN, VSYNC and HSYNC Waveforms

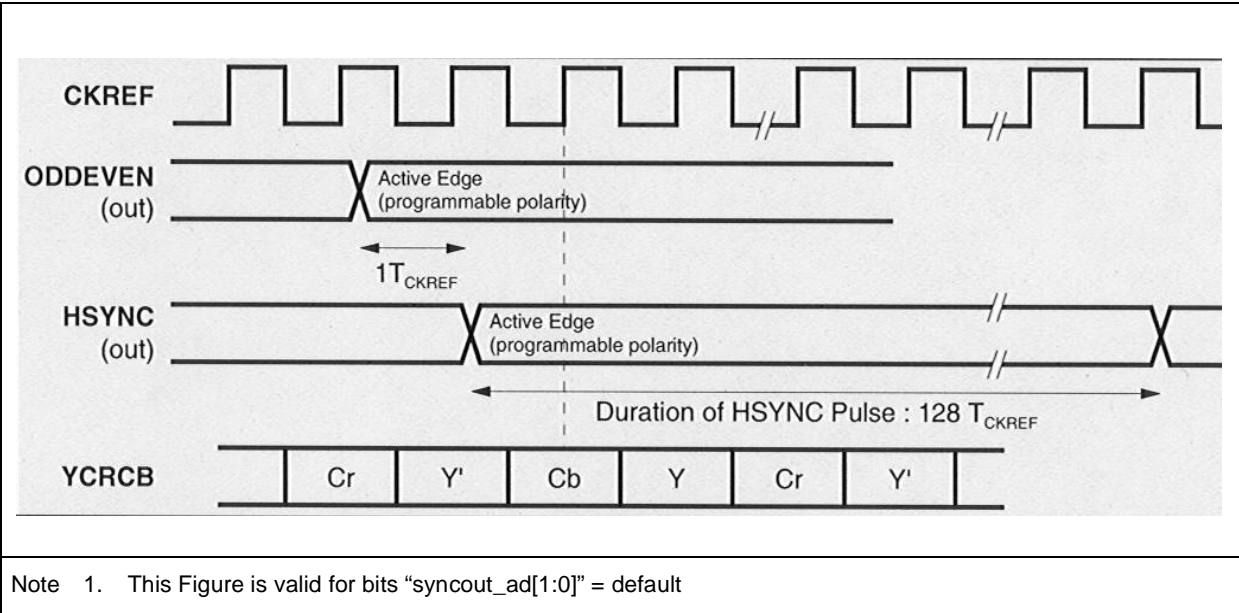


Figure 16-3. Master Mode Sync Signals

16.2.5. SLAVE MODES

Five slave modes are available:

- 1) ODDEV+HSYNC based (line-based sync)
- 2) VSYNC+HSYNC based (another type of line-based sync)
- 3) ODDEV-only based (frame-based sync)
- 4) VSYNC-only based (another type of frame-based sync)
- 5) Sync-in-data based (line locked or frame locked)

ODDEV refers to an odd/even field flag (also known as not-top/bottom), HSYNC is a line sync signal, VSYNC is a vertical sync signal. The waveforms are depicted in [Figure 16-2](#).

The polarities of HSYNC and VSYNC/ODDEV are independently programmable in all slave modes.

16.2.6. HSYNC+ODDEV BASED LINE SYNCHRONIZATION

Synchronization is performed on a line-by-line basis by locking onto incoming ODDEV and HSYNC signals. Refer to Figure 11 for waveforms and timings. The polarities of the active edges of HSYNC and ODDEV are programmable and independent.

The first active edge of ODDEV initialises the internal line counter but encoding of the first line does not start until an HSYNC active edge is detected. At the earliest, HSYNC may transition at the same time as ODDEV. At that point, the internal sample counter is initialised and encoding of the first line starts. Then, encoding of each subsequent line is individually triggered by HSYNC active edges. The phase relationship between HSYNC and the incoming YCrCb data is normally such that the first clock rising edge following the HSYNC active edge samples "Cb" (i.e. a 'blue' chroma sample within the YCrCb stream). It is however possible to internally delay the incoming sync signals (HSYNC+ODDEV) by up to three clock cycles to cope with different data/sync phasings, using configuration bits "Syncin_ad" (Reg. 4, see [Section 16.6.5](#).)

The TV Output Port is thus fully slaved to the HSYNC signal, which means that lines may contain more or less samples than typical 525/625 system requirement.

If the digital line is shorter than its nominal value, the sample counter is re-initialised when the 'early' HSYNC arrives and all internal synchronization signals are re-initialised.

If the digital line is longer than its nominal value, the sample counter is stopped when it reaches its nominal end-of-line value and waits for the 'late' HSYNC before reinitializing.

The field counter is incremented on each ODDEV transition. The line counter is reset on the HSYNC following each active edge of ODDEV.

16.2.7. HSYNC+VSYNC BASED LINE SYNCHRONIZATION

Synchronization is performed on a line-by-line basis by locking onto incoming VSYNC and HSYNC signals. The polarities of HSYNC and VSYNC are programmable and independent. The incoming VSYNC signal is immediately transformed into a waveform identical to the odd/even waveform of an ODDEV signal. The behaviour of the core is therefore identical to that described above for ODDEV+HSYNC based synchronization. Again, the phase relationship between HSYNC and the incoming YCrCb data is normally such that the first clock rising edge following the HSYNC active edge samples "Cb" (i.e. a 'blue' chroma sample within the YCrCb stream). It is however possible to internally delay the incoming sync signals (HSYNC+VSYNC) by up to three clock cycles to cope with different data/sync phasings, using configuration bits "Syncin_ad" (Reg. 4, see [Section 16.6.5.](#)) The field counter is incremented on each active edge of VSYNC.

16.2.8. ODDEV-ONLY BASED FRAME SYNCHRONIZATION

Synchronization is performed on a frame-by-frame basis by locking onto an incoming ODDEV signal. A line sync signal is derived internally and is also output as HSYNC. The phase relationship between ODDEV and the incoming YCrCb data is normally such that the first clock rising edge following the ODDEV active edge samples "Cb" (i.e. a 'blue' chroma sample within the YCrCb stream). It is however possible to internally delay the incoming ODDEV signal by up to three clock cycles to cope with different data/sync phasings, using configuration bits "Syncin_ad" (Reg. 4 - see [Section 16.6.5.](#)).

The first active edge of ODDEV triggers generation of the analog sync signals and encoding of the incoming video data. As frames are expected to be constant in duration, the next ODDEV active transition is expected at a precise time after the last ODDEV was detected. So, once an active ODDEV edge has been detected, checks are made to ensure that following ODDEV are present at the expected times.

Encoding and analog sync generation carry on unless three successive check failures occur, in which case, one of three resulting actions is possible, according to the programmed configuration (Reg. 1-2, see [Section 16.6.2.](#) and [Section 16.6.3.](#)):

- 1) If 'free-run' is enabled, the TV Output Port carries on outputting the digital line sync HSYNC and generating analog video, just as though the expected ODDEV edge had been present. However, it will re-synchronise onto the next ODDEV active edge detected, whatever its location.
- 2) If 'free-run' is disabled but bit 'sync_ok' is set in configuration register1, the TV Output Port sets the active portion of the TV line to the black level but carries on outputting the analog sync tips (on Ys and CVBS) and the digital line sync signal HSYNC. (When programmed, AGC pulses are also present in the analog sync waveform).
- 3) If 'free-run' is disabled and the bit 'sync_ok' is not set, all analog video is at black level and neither analog sync tips nor digital line sync are output.

Note that this mode is a frame-based sync mode, as opposed to a field-based sync mode, that is, only one type of edge (rising or falling, according to bit 'polv' in Reg. 0, - see [Section 16.6.1.](#)) is of interest to the TV Output Port, the other one is ignored.

16.2.9. VSYNC ONLY BASED FRAME SYNCHRONIZATION

Synchronization is performed on a frame-by-frame basis by locking onto an incoming VSYNC signal. An auxiliary line sync signal HSYNC must also be fed to the TV Output Port, which uses it to reconstruct from VSYNC and HSYNC information an internal odd/even waveform identical to that of an ODD-EVEN signal. Therefore the behaviour of the core is identical to that described above for ODDEVEN only based synchronization (except that nothing is output on HSYNC pin since it is an input port in that mode).

Note that HSYNC is an input but has no other use than allowing the TV Output Port to decide whether an incoming VSYNC pulse flags an odd or an even field. In other words, the TV Output Port does not lock onto HSYNC in this mode since this is NOT a line-locked mode.

The phase relationship between VSYNC and the incoming YCrCb data is normally such that the first clock rising edge following the VSYNC active edge samples "Cb" (i.e. a 'blue' chroma sample within the YCrCb stream). It is however possible to internally delay the incoming sync signals (VSYNC+HSYNC) by up to three clock cycles to cope with different data/sync phasings, using configuration bits "Syncin_ad" (Reg. 4).

16.2.10. 'END-OF-FRAME' WORD BASED DATA-EMBEDDED SYNCHRONIZATION

Synchronization is performed by extracting the 1-to-0 transitions of the 'F' flag (end-of-frame) from the 'EAV' (End-of-Active Video) sequence embedded within ITU-R656/D1 compliant digital video streams. Both a frame sync signal and a line sync signal are derived and are made available externally as ODDEVEN and HSYNC.

The first successful detection of the 'F' flag triggers generation of the analog sync signals and encoding of the incoming video data. As frames are expected to be of constant duration, the next EAV word containing the 'F' flag is expected at a precise time after the latest detection.

So, once an active 'F' flag has been detected, checks are made to see whether the following flags are present within the incoming video stream at the expected times.

Encoding and analog sync generation carry on unless three successive check failures occur, in which case, one of three resulting actions is possible, according to the programmed configuration:

- 1) If 'free-run' is enabled, the TV Output Port continues to generate the digital frame and line syncs (ODD-EVEN and HSYNC) and generates analog video just as though the expected 'F' flag had been present. However, it will re-synchronise onto the next 'F' flag detected within the incoming CCIR656/D1 video stream.
- 2) If 'free-run' is disabled but the bit 'sync_ok' is set in the configuration registers, the TV Output Port sets the active portion of the TV line to the black level but carries on outputting the analog sync tips (on Ys and CVBS) and the digital frame and line sync signals ODDEVEN and HSYNC (when programmed, AGC pulses are also present in the analog sync waveform).
- 3) If 'free-run' is disabled and the bit 'sync_ok' is not set, all analog video is at the black level and neither analog sync tips nor digital frame/line sync are output.

The SAV and EAV words are Hamming-decoded. After detection of two successive errors, a bit is set in the status register to inform the micro-controller of the poor transmission quality.

TV OUTPUT PORT

16.2.11. 'END-OF-LINE' WORD BASED DATA-EMBEDDED SYNCHRONIZATION

Synchronization is performed by extracting the 'F' and 'H' flags from the 'SAV' (Start of Active Video) and 'EAV' (End of Active Video) words embedded within ITU-R656/D1 compliant digital video streams.

A line sync signal and a frame sync signal are derived internally from these flags and are output on the HSYNC and ODDEVEN/VSYNC pins in output mode. These signals are also exploited by the core of the circuit which treats them as incoming ODDEVEN and HSYNC signals in HSYNC+ODDEV based synchronization.

16.2.12. INPUT DEMULTIPLEXER

The incoming 27 Mbit/s YCrCb data is demultiplexed into a 'blue-difference' chroma information stream, a 'red-difference' chroma information stream and a luma information stream. Incoming data bits are treated as blue, red or luma samples, according to their relative position with respect to the sync signals in use and to the content of configuration bits "Syncin_ad" (slave modes) or "Syncout_ad" (master mode).

The ITU-R601 recommendation defines the black luma level as $Y = 16\text{dec}$ and the maximum white luma level as $Y = 235\text{dec}$. Similarly, it defines 225 quantization levels for the colour difference components (Cr, Cb), centred around 128.

Accordingly, incoming YCrCb samples can be saturated in the input multiplexer with the following rules:

for Cr or Cb samples:

$Cr, Cb > 240 \Rightarrow Cb \text{ saturated at } 240$

$Cr, Cb < 16 \Rightarrow Cr, Cb \text{ saturated at } 16$

for Y samples:

$Y > 235 \Rightarrow Y \text{ saturated at } 235$

$Y < 16 \Rightarrow Y \text{ saturated at } 16$

This avoids having to heavily saturate the composite video codes before digital-to-analog conversion in case erroneous or unrealistic YCrCb samples are input to the encoder (there may otherwise be overflow errors in the codes driving the DACs), and therefore avoids generating a distorted output waveform.

However, in some applications, it may be desirable to let 'extreme' YCrCb codes pass through the demultiplexer. This is also possible, provided that bit "maxdyn" is set in configuration register 6 (see [Section 16.6.7](#)). In this case, only codes 00h and FFh are overridden. If such codes are found in the active video samples, they are forced to 01h and FEh.

In any case, the YCrCb codes are not overridden for EAV/SAV decoding.

The demultiplexer is also able to handle 54 Mbit/s YCrCb streams for dual encoding applications. Refer to the STV0119A PAL/NTSC High Performance Digital Encoder Data Sheet, Section IV.17, Dual Encoding Application 54 Mbit/s YCrCb Interface, for further details.

16.2.13. SUB-CARRIER GENERATION

A Direct Digital Frequency Synthesiser (DDFS) using a 24-bit phase accumulator, generates the required colour sub-carrier frequency. This oscillator feeds a quadrature modulator which modulates the baseband chrominance components. The sub-carrier frequency is obtained from the following equation:

$$F_{sc} = (24\text{-bit Increment Word} / 2^{24}) \times CKREF$$

Hardwired Increment Word values are available for each standard (except for 'NTSC-4.43') and can be selected automatically.

Alternatively (according to bit `selrst' in Reg. 2.), the frequency can be fully customised by programming other values into a dedicated Increment Word Register (Reg. 10-11-12). This allows, for instance, the encoding of "NTSC-4.43" or "PAL-M-4.43".

This is done using the following procedure:

- Program the required increment in Registers 10 to 12.
- Set bit `selrst' to `1' in Configuration Register 2.
- Perform a software reset (Reg. 6).

Caution: This sets back all bits from Reg. 7 onwards to their default value, when they can be reset.

Warning: If a standard change occurs after the software reset, the increment value is automatically re-initialised with the hardwired or loaded value according to bit selrst.

The reset phase of the colour sub-carrier can also be software-controlled (Reg. 13-14). The sub-carrier phase can be periodically reset to its nominal value to compensate for any drift introduced by the finite accuracy of the calculations. Sub-carrier phase adjustment can be performed every line, every eight field, every four field, or every two field (Register 2 bits valrst[1:0]).

16.2.14. BURST INSERTION

The colour reference burst is inserted so as to always start with a positive zero crossing of the subcarrier sine wave.

The first and last half-cycles have a reduced amplitude so that the burst envelope starts and ends smoothly.

The burst contains 9 or 10 sinewave cycles of 4.43361875 MHz or 3.579545 MHz according to the standard programmed in the Control Register (Reg. 0, bits std[1:0]), as follows:

NTSC-M	9 cycles of 3.579542 MHz
PAL-BDGIH	10 cycles of 4.43361875 MHz
PAL-M	9 cycles of 3.57561149 MHz
PAL-N	9 cycles of 3.5820558 MHz

It is possible to turn the burst off (no burst insertion) by setting configuration bit `bursten' to 0 (register2).

Notes :

- 1) Two strategies exist for burst insertion: one is to merely gate and shape the subcarrier for burst insertion, the other is more elaborate and is to always start the burst with a positive-going zero crossing. In the first case the phase of the subcarrier when the burst starts is not controlled, with the consequence that some of its first and last cycles are more heavily distorted. The second solution guarantees smooth start and end of burst with a maximum of undistorted burst cycles and can only be beneficial to chroma decoders. This is the solution implemented in the TV Output Port.
- 2) While the first option gave constant burst start time but uncontrolled initial burst phase, the second solution guarantees start on a positive-going zero crossing with the consequence that two burst start locations are visible over successive lines, according to the line parity. This is normal and explained below.
- 3) In NTSC, the relation between subcarrier frequency and line length creates a 180° subcarrier phase difference (with respect to the horizontal sync) from one line to the next according to the line parity. So if the burst always starts with the same phase (positive-going zero crossing), this means the burst will be inserted at time X or at time $X + T_{NTSC}/2$ after the horizontal sync tip according to the line parity, where T_{NTSC} is the duration of one cycle of the NTSC burst.

TV OUTPUT PORT

4) With PAL, a similar rationale holds, and again there will be two possible burst start locations. The subcarrier phase difference (with respect to the horizontal sync) from one line to the next in that case is either 0 or 180° with the following series: A-A-B-B-A-A-...-etc. where A denotes 'A-type' bursts and B denotes 'B-type' bursts, A-type and B-type being 180° out of phase with respect to the horizontal sync. So two locations are possible, one for A-type, the other for B-type.

5) This assumes a periodic reset of the subcarrier is automatically performed (see bits `valrst[1:0]` in Reg 2). Otherwise, over several frames, the start of burst will drift within an interval of one subcarrier cycle. THIS IS NORMAL and means the burst is correctly locked to the colours encoded. The equivalent effect with a gated burst approach would be the following: the start location would be fixed but the phase with which the burst starts (with respect to the horizontal sync) would be drifting.

16.2.15. LUMINANCE ENCODING

The demultiplexed Y samples are band-limited and interpolated at CKREF clock rate. The resulting luminance signal is properly scaled before insertion of any Closed-captions, CGMS or Teletext data and synchronization pulses.

The interpolation filter compensates for the $\sin(x)/x$ attenuation inherent to D/A conversion and greatly simplifies the output stage filter. In addition, the luminance that is added to the chrominance to create the composite CVBS signal can be trap-filtered at 3.58 MHz (NTSC) or 4.43 MHz (PAL). This allows to cope with application oriented towards low-end TV sets which are subject to cross-colour if the digital source has a wide luminance bandwidth (e.g. some DVD sources). Note that the trap filter does not affect the S-VHS luminance output nor the RGB outputs.

A 7.5 IRE pedestal can be programmed if needed with all standards (see Reg1, bit setup). This allows in particular to encode Argentinian and non-Argentinian PAL-N, or Japanese NTSC (NTSC with no setup).

A programmable delay can be inserted on the luminance path to compensate any chroma/luma delay introduced by off-chip filtering (chroma and luma transitions being coincident at the DAC output with default delay) (Reg3, bits `del[2:0]`).

16.2.16. CHROMINANCE ENCODING

U and V chroma components are computed from demultiplexed Cb, Cr samples. Before modulating the subcarrier, these are band-limited and interpolated at CKREF clock rate. This processing eases the filtering following D/A conversion and allows a more accurate encoding. A set of four different filters is available for chroma filtering to fit a wide variety of applications in the different standards and include filters recommended by ITU-R Rec624-4 and SMPTE170-M. The available 3dB bandwidths are 1.1, 1.3, 1.6 or 1.9 MHz (Reg1, bits `flt[1:0]`).

The narrower bandwidths are useful against cross-luminance artefacts, the wider bandwidths allow the retention of higher chroma contents and consequently produce improved image quality.

16.2.17. COMPOSITE VIDEO SIGNAL GENERATION

The composite video signal is created by adding the luminance (after optional trap filtering, Reg 3 bits `entrap` and `trap_pal`) and the chrominance components. A saturation function is included in the adder to avoid overflow errors should extreme luminance levels be modulated with highly saturated colours (this does not correspond to natural colours but may be generated by computers or graphic engines).

A 'colour killing' function is available (Reg 1, bit `coki`) whereby the composite signal contains no chrominance, i.e. replicates the trap-filtered luminance. Note that this function does not suppress the chrominance on the S-VHS outputs (nevertheless suppressing the S-VHS chrominance is possible using bit "`bkg_c`" in Reg 5).

16.2.18. RGB ENCODING

After demultiplexing, the Cr and Cb samples feed a four times interpolation filter. The resulting baseband chroma signal has a 2.45 MHz bandwidth and is combined with the filtered luma component to generate R, G, B samples at 27 MHz.

16.2.19. CLOSED CAPTIONING

Closed-captions (or data from an Extended Data Service as defined by the Closed-Captions specification) can be encoded by the circuit. The closed caption data is delivered to the circuit through the writing the data to User registers 39 and 40. Two dedicated pairs of bytes (two bytes per field), each pair preceded by a clock run-in and a start bit can be encoded and inserted on the luminance path on a selected TV line. The Clock Run-In and Start code are generated by the TV Output Port.

Closed-caption data registers are double-buffered so that loading can be performed any time, even during line 21/284 or any other selected line.

User register 39 (resp. 41) contains the first byte to send (LSB first) after the start bit on the appropriate TV line in field 1 (resp. field 2), and user register 40 (resp. 42) contains the second byte to send. The TV line number where data is to be encoded is programmable (Reg. 37, 38). Lines that may be selected include those used by the StarSight data broadcast system. Closed-caption data has priority over any CGMS or signals programmed for the same line.

The internal Clock Run-In generator is based on a Direct Digital Frequency Synthesiser. The nominal instantaneous data rate is 503.5 kbit/s (i.e. 32 times the NTSC line rate). Data LOW corresponds nominally to 0 IRE, data HIGH corresponds to 50 IRE at the DAC outputs.

When closed-captioning is on (bits cc1/cc2 in Reg.1), the CPU should load the relevant registers (reg. 39 and 40, or 41 and 42) once every frame at most (although there is in fact some margin due to the double-buffering). Two bits are set in the status register in case of attempts to load the closed-caption data registers too frequently, these can be used to regulate loading rate.

The closed caption encoder considers that closed caption data has been loaded and is valid on completion of the write operation into register 40 for field1, into register 42 for field 2. If closed caption encoding has been enabled and no new data bytes have been written into the closed caption data registers when the closed caption window starts on the appropriate TV line, then the circuit outputs two US-ASCII NULL characters with odd parity after the start bit.

16.2.20. CGMS ENCODING

CGMS (Copy Generation Management System -also known as VBID and described by standard CPX-1204 of EIAJ) data can be encoded by the circuit. Three bytes (20 significant bits) are to be written by the user into User Registers 31, 32 and 33. Two reference bits ('1' then '0') are encoded first, followed by 20 bits of CGMS data (including a Cyclic Redundancy Check sequence, not computed by the device and supplied to it as part of the 20 data bits). The reference bits are generated locally by the TV Output Port.

When CGMS encoding is enabled, the CGMS (see bit encgms in Reg 3) waveform is continuously present once in each field, on lines 20 and 283 (SMPTE-525 line numbering). The CGMS data register is double-buffered, which means that it can be loaded any time (even during line 20/283) without any risk of corrupting CGMS data that could be in the process of being encoded. The CGMS encoder considers that new CGMS data has been loaded and is valid on completion of the write operation into register 33.

16.2.21. LINE SKIP / LINE INSERT CAPABILITY

This patented feature of the TV Output Port offers the possibility to cut the cost of the application by suppressing the need for a VCXO.

Ideally, the master clock used on the application board and fed to the MPEG decoding IC would have exactly same frequency as the clock that was used when the MPEG data was encoded. Obviously this is

TV OUTPUT PORT

not realistic; up to now a solution commonly chosen is to dynamically adjust the clock on the board as close to the 'ideal' clock as possible with the help of time stamps embedded within the MPEG stream. Such tracking often involves the use of a VCXO: when the MPEG data buffer fills up to more than a preset threshold, the clock frequency is increased; when it empties down below a lower threshold, the clock frequency is lowered.

The TV Output Port offers an alternative, cost-saving solution: by programming the two bits jump and dec_ninc in configuration Reg6, the TV Output Port is able to reduce or increase the length of some frames in a way that will not introduce visible artefacts (even if comb-filtering is used). These bits should be set according to the level of the MPEG data buffer. Refer to Register 6, Register 9 and Registers 21-22-23 in the TV Output Port Chapter for a complete bit description.

Operation with the TV Output Port as sync master is as follows:

- 1) If the MPEG data buffer fills up too much: set bit "jump" to '1' and bit "dec_ninc" to '1'. The TV Output Port will reduce the length of the current frame (Bit "jump" will then automatically be reset to '0').
- 2) If the MPEG data buffer empties too much: set bit "jump" to '1' and bit "dec_ninc" to '0'. The TV Output Port will increase the length of the current frame (Bit "jump" will then automatically be reset to '0').

These operations can be repeated until the MPEG data buffer is inside its fixed limits. It is also possible to use the line skip/repeat capability in non-interlaced mode.

This functionality of the TV Output Port is also available in slave mode. In this case, the sync signals supplied to the TV Output Port must be in accordance with the modified frame lengths programmed.

16.2.22. CVBS, S-VHS AND RGB ANALOG OUTPUTS

Four out of six video signals (composite CVBS, S-VHS (Y/C) and RGB) can be directed to four analog output pins through 9-bit D/A converters operating at the reference clock frequency.

The available combinations (see [Section 12.9.33](#), bit 3) are:

S-VHS (Y/C) + CVBS + CVBS1 when bit 3 is set to '1'

or : R, G, B + CVBS1 when bit3 is set to 0.

A single external analog power supply pair is used for all DACs, but two independent pairs of current and voltage references are needed. Each current reference pin is normally connected externally to a resistor tied to the analogue ground, while each voltage reference pin is normally connected to a capacitance tied to analogue ground.

The internal current sources are independent from the positive supply, thanks to a bandgap, and the consumption of the DACs is constant whatever the converted codes.

Any unused DAC may be independently disabled by software, in which case its output is at 'neutral' level (blanking for luma and composite outputs, no colour for chroma output, black for RGB outputs). For applications where a single CVBS output is required, the RGB/CVBS+S-VHS Triple DAC should be disabled and Pins $I_{REF(RGB)}$, VR_RGB tied to analog power supply.

16.3. TV OUTPUT PORT REGISTER ACCESS

The TV Output Port Registers are memory mapped to the 4 MBytes which are reserved for Graphics and Video. The TV Output Port Address Map is described below.

As GBASE is usually set to 1000 (Default value), the base address to access the TV Output Port Space is 084CA000h. Note that this is only applicable if GBASE is 1000.

Bits 31-28, These bits should be set to '0'.

Bits 27-24, **GBase**, These bits are determined by the GBase Register in [Section 12.9.8](#).

Bits 23-12, **TV Output Port Base Register Address**, These bits must be set to CAh.

Bits 11-0, **TV Output Port Register Select**, The location and access to these registers is given in Table 16-5.

Bits 31-28	Bits 27-24	Bits 23-20	Bits 19-12	Bits 11-0
0000	GBASE	0100	1100 1010	Register Address

16.4. TV OUTPUT PORT REGISTERS

Table 16-5. TV Output Port Register/Bit Mapping

Register		Index	MSB							LSB	
Configuration(0)	R/W	00h	std1	std0	sync2	sync1	sync0	polh	polv	freerun	
Configuration(1)	R/W	01h	blki	flti	flt0	sync_ok	coli	setup	cc2	cc1	
Configuration(2)	R/W	02h	nintrl	enrst	bursten	set_4:4:4	selrst	rstosc_b uf	valrst1	x	
Configuration(3)	R/W	03h	entrap	trap_4.43	encgms	ck_in_pha se	del2	del1	del0	x	
Configuration(4)	R/W	04h	syncin_ad 1	syncin_a d0	synoutc_ ad1	synoutc_a d0	aline	del42	del41	del40	
Configuration(5)	R/W	05h	selrst_inc	bkdac1	bkdac2	bkdac3	bkdac4	bkdac5	bkdac6	dacinv	
Configuration(6)	R/W	06h	softreset	jump	dec_ninc	free_jump	cfc1	cfc0	x	maxdyn	
Reserved(7)	x	07h	x	x	x	x	x	x	x	x	
Configuration(8)	R/W	08h	ph_rst_m od1	ph_rst_m od0	conf_out 1	conf_out0	blk_all	x	x	x	
Status (9)	R	09h	hok	atfr	b2_free	b1_free	fieldct2	fieldct1	fieldct0	jumping	
Increment_dfs(10)	R/W	0Ah	d23	d22	d21	d20	d19	d18	d17	d16	
Increment_dfs(11)	R/W	0Bh	d15	d14	d13	d12	d11	d10	d9	d8	
Increment_dfs(12)	R/W	0Ch	d7	d6	d5	d4	d3	d2	d1	d0	
Phase_dfs(13)	R/W	0Dh	-	-	-	-	-	-	o23	o22	
Phase_dfs(14)	R/W	0Eh	o21	o20	o19	o18	o17	o16	o15	o14	
Reserved(15)	x	0Fh	x	x	x	x	x	x	x	x	
Reserved(16)	x	10h	x	x	x	x	x	x	x	x	
Reserved(17)	R	11h	0	1	1	1	0	1	1	1	
Reserved(18)	R	12h	0	0	0	0	0	0	0	1	
Reserved(19)	x	13h	x	x	x	x	x	x	x	x	
Reserved(20)	x	14h	x	x	x	x	x	x	x	x	
line_reg(21)	R/W	15h	ltarg8	ltarg7	ltarg6	ltarg5	5ltarg4	ltarg3	ltarg2	ltarg1	
line_reg(22)	R/W	16h	ltarg0	lref8	lref7	lref6	lref5	lref4	lref3	lref2	
line_reg(23)	R/W	17h	lref1	lref0	-	-	-	-	-	-	
cgms_bit_1-4(31)	R/W	1Fh	-	-	-	-	bit1	bit2	bit3	bit4	
cgms_bit_5-12(32)	R/W	20h	bit5	bit6	bit7	bit8	bit9	bit10	bit11	bit12	
cgms_bit_13-20(33)	R/W	21h	bit13	bit14	bit15	bit16	bit17	bit18	bit19	bit20	
Reserved(34)	x	22h	x	x	x	x	x	x	x	x	
...	x	...									
Reserved(38)	x	26h	x	x	x	x	x	x	x	x	
c.c.c.F1(39)	R/W	27h	opc11	c117	c116	c115	c114	c113	c112	c111	
c.c.c.F1(40)	R/W	28h	opc12	c127	c126	c125	c124	c123	c122	c121	

TV OUTPUT PORT

Table 16-5. TV Output Port Register/Bit Mapping (cont'd)*

Register		Index	MSB							LSB	
c.c.c.F2(41)	R/W	29h	opc21	c217	c216	c215	c214	c213	c212	c211	
c.c.c.F2(42)	R/W	2Ah	opc22	c227	c226	c225	c224	c223	c222	c221	
cclif1(43)	R/W	2Bh	x	x	x	l1_4	l1_3	l1_2	l1_1	l1_0	
cclif2(44)	R/W	2Ch	x	x	x	l2_4	l2_3	l1_1	l1_1	l1_0	
Reserved(45)	x	2Dh	x	x	x	x	x	x	x	x	
...	x	...									
Reserved(63)	x	3Fh	x	x	x	x	x	x	x	x	

16.6. TV OUTPUT PORT REGISTER CONTENTS AND DESCRIPTION

16.6.1. REGISTER_0 - CONFIGURATION 0

Config_0

Access = 84CA000h

Regoffset = 000h

7	6	5	4	3	2	1	0
std		sync			polh	polv	freerun
Default value after reset = 0X92h							

Bit Number	Mnemonic	Description
Bits 7-6	std	Standard Selected, std[1-0] (see Table 16-1). Note: Standard on hardware reset is NTSC; any standard modification selects automatically the right parameters for correct subcarrier generation.
Bits 5-3	sync	Configuration, sync[2-0] (see Table 16-2). Caution: In VSYNC-only based slave mode (sync[2:0]="100"), HSYNC is nevertheless needed as an input.
Bit 2	polh	Synchro H, polh. Active edge of HSYNC selection (when input) or polarity of HSYNC (when output) 0: HSYNC is a negative pulse (128 T _{CKREF} wide) or falling edge is active 1: HSYNC is a positive pulse (128 T _{CKREF} wide) or rising edge is active
Bit 1	polv	Synchro V, polv. Active edge of ODDEVEN/VSYNC selection (when input) or polarity of ODDEV (when output). 0: Falling edge of ODDEVEN flags start of field1 (odd field) or VSYNC is active low 1: Rising edge of ODDEVEN flags start of field1 (odd field) or VSYNC is active high Note: In master mode: polarity of ODDEVEN output. In slave by F (from EAV) : polv = 0 (cf D1 encoding) and ODDEVEN polarity is the image of F extracted from EAV words.
Bit 0	freerun	Freerun, freerun. 0: Disabled 1: Enabled Caution: This bit is taken into account in ODDEV-only, VSYNC-only or 'F' based slave modes and is irrelevant to other synchronization modes.

Table 16-1. Standard Selected

std1	std0	Standard Selected
0	0	PAL BDGHI
0	1	PAL N (see bit setup)
1	0	NTSC M
1	1	PAL M

TV OUTPUT PORT

Table 16-2. Sync Configuration

sync2	sync1	sync0	Configuration
0	0	0	ODDEVEN based SLAVE mode (frame locked)
0	0	1	F only based SLAVE mode (frame locked)
0	1	0	ODDEV+HSYNC based SLAVE mode (line locked)
0	1	1	'F'+ 'H' based SLAVE mode (line locked)
1	0	0	VSYNC-only based SLAVE mode (frame locked) (see Note)
1	0	1	VSYNC+HSYNC based SLAVE mode (line locked)
1	1	0	MASTER mode
1	1	1	AUTOTEST mode (colour bar pattern)

16.6.2. REGISTER_1 - CONFIGURATION 1

Config_1

Access = 84CA000h

Regoffset = 001h

7	6	5	4	3	2	1	0
blkli	flt1	flt0	sync_ok	coki	setup	cc2	cc1
Default value after reset = 0x44h							

Bit Number	Mnemonic	Description
Bit 7	blkli	<p>Vertical Blanking Interval selection for active video, blkli. Blanking lines area).</p> <p>0: ('partial blanking') Only following lines inside Vertical Interval are blanked NTSC-M: lines [1..9], [263(half)..272] (525-SMPTE) PAL-M: lines [523..6], [260(half)..269] (525-CCIR) other PAL: lines [623(half)..5], [311..318] (625-CCIR) This mode allows preservation of VBI data embedded within incoming YCrCb, e.g. Wide Screen signalling (full line 23), Video Programming Service (line16), etc.)</p> <p>1: ('full blanking') All lines inside VBI are blanked NTSC-M: lines [1..19], [263(half)..282] (525-SMPTE) PAL-M: lines [523..16], [260(half)..279] (525-CCIR) other PAL: lines [623(half)..22], [311..335] (625-CCIR) Note: blkli must be set to '0' when closed captions and are to be encoded on following lines: 525/60 system: before line 20(SMPTE) or before line 283(SMPT 625/50 system: before line 23(CCIR) or before line 336(CCIR) For CGMS and Teletext encodings, blkli value is not taken into account.</p>
Bits 6-5	flt	U/V Chroma filter bandwidth selection (see Table 16-3)
Bit 4	sync_ok	<p>Sync Ok, sync_ok. Availability of sync signals (analog and digital) in case of input synchronization loss with no free-run active (i.e. freerun='0').</p> <p>0: No synchro output signals 1: Output synchros available on YS, CVBS and, when applicable, HSYNC (if output port), ODDEVN (if output port), i.e same behaviour as free-run except that video outputs are blanked in the active portion of the line. Caution: This bit is taken into account in ODDEV-only, VSYNC-only or 'F' based slave modes and is irrelevant to other synchronization modes.</p>
Bit 3	coki	<p>Colour killer, coki</p> <p>0: Colour ON 1: Colour suppressed on CVBS (and CVBS1) output signal (CVBS=YS) but colour still present on C and RGB outputs. For colour suppression on chroma DAC 'C', see register 5 bit bkg_c.</p>
Bit 2	setup	<p>Pedestal enable, setup.</p> <p>0: Blanking level and black level are identical on all lines (e.g.: Argentinian PAL-N, Japan NTSC-M, PAL-BDGH1) 1: Black level is 7.5 IRE above blanking level on all lines outside VBI (e.g. Paraguayan and Uruguayan PAL-N) In all standards, gain factor is adjusted to obtain the required levels for chrominance.</p>
Bits 1-0	cc	Closed caption encoding mode (see Table 16-4)

TV OUTPUT PORT

Table 16-3. U/V Chroma Filter Bandwidth

Bit 6 flt1	Bit 5 flt0	3dB Bandwidth	Typical Application
0	0	f-3 = 1.1 MHz	Low definition NTSC filter
0	1	f-3 = 1.3 MHz	Low definition PAL filter
1	0	f-3 = 1.6 MHz	High definition NTSC filter (ATSC compliant) & PAL M/N (ITU-R 624.4 compliant)
1	1	f-3 = 1.9 MHz	High definition PAL filter: Rec 624 - 4 for PAL BDG/I compliant

Table 16-4. Closed Caption Encoding Mode

Bit 1 cc2	Bit 2 cc1	Encoding Mode
0	0	No closed caption/extended data encoding
0	1	Closed caption/extended data encoding enabled in field 1 (odd)
1	0	Closed caption/extended data encoding enabled in field 2 (even)
1	1	Closed caption/extended data encoding enabled in both fields

16.6.3. REGISTER_2 - CONFIGURATION 2

Config_2

Access = 84CA000h

Regoffset = 002h

7	6	5	4	3	2	1	0
nintrl	enrst	bursten	Set4:4:4	selrst	rstocs_buf	valrest1	valrst0
Default value after reset = 0x20h							

Bit Number	Mnemonic	Description
Bit 7	nintrl	Non-interlaced mode select, nintrl. 0: Interlaced mode (625/50 or 525/60 system) 1: Non-interlaced mode(2x312/50 or 2x262/60 system) Note: 'nintrl' update is internally taken into account on beginning of next frame.
Bit 6	enrst	Cyclic update of DDFS phase, enrst. 0: No cyclic subcarrier phase reset 1: Cyclic subcarrier phase reset depending of valrst1 and valrst0 (see below)
Bit 5	bursten	Chrominance burst control, bursten. 0: Burst is turned off on CVBS (and CVBS1), C and RGB outputs are not affected 1: Burst is enabled
Bit 4	Set4:4:4	Set4:4:4 Selects the inputs for RGB and YUV (Y Cr Cb) encoding. 0: YCrCb Input (4:2:2) 1: Y and CrCb Input (4:4:4)
Bit 3	selrst	Select set of reset values for Direct Digital Frequency Synthesiser, selrst. 0: Hardware reset values for phase and increment of subcarrier oscillator 1: Loaded reset values selected (see contents of Registers 10 to 14)
Bit 2	rstocs_buf	Software phase reset of DDFS (Direct Digital Frequency Synthesiser) buffer. 0: Inactive 1: When a 0-to-1 transition occurs either the hardwired default phase value or the value loaded in Reg. 13-14 (according to bit 'selrst') is put to the phase buffer. This value is then loaded into accumulator (phase of sub-carrier) when the bits 'ph_rst_osc' from Register 8 are programmed or when standard changes or softreset occurs. Note: Bit 'rstosc_buf' is automatically set back to '0' after the buffer is loaded.
Bits 1-0	valrest	Oscillator Value Reset, valrst[1-0]. (See Table 16-5) Note: valrst[1-0] is taken into account only if bit 'enrst' is set. Resetting the oscillator means forcing the value of the accumulator phase to its nominal value to avoid accumulating errors due to the finite number of bits used internally. The value to which the accumulator is reset is either the hardwired default phase value or the value loaded in Register 13-14 (according to bit 'selrst'), to which a 0x, 90x, 180x, or 270x correction is applied according to the field and line on which the reset is performed.

Table 16-5. Oscillator Reset Value

valrst1	valrst0	Selection
0	0	Automatic reset of the oscillator every line
0	1	Automatic reset of the oscillator every 2nd field
1	0	Automatic reset of the oscillator every 4th field
1	1	Automatic reset of the oscillator every 8th field

16.6.4. REGISTER_3 - CONFIGURATION 3

Config_3

Access = 84CA000h

Regoffset = 003h

7	6	5	4	3	2	1	0
entrap	pal_4.43	encgms	nosd	del2	del1	del0	Rsv
Default value after reset = 00000000h							

Bit Number	Mnemonic	Description
Bit 7	entrap	Enable trap filter, entrap. 0: Trap filter disabled 1: Trap filter enabled
Bit 6	pal_4.43	Trap Filter Select, pal_4.43. 0: To select the trap filter centred around 3.58 MHz 1: To select the trap filter centred around 4.43 MHz Note: 'trap_pal' is taken into account only if bit 'entrap' is set.
Bit 5	encgms	CGMS encoding enable, encgms. 0: Disabled 1: Enabled Note: When encgms is set to '1' Closed-Captions/Extended Data Services should not be programmed on lines 20 and 283 (525/60, SMPTE line number convention).
Bit 4	nosd	CKREF Actif Edge Select, nosd. Choice of active edge of 'ckref' (master clock) that samples incoming YCrCb data. 0: 'ckref' rising edge (e.g. data with OSD coming from STi3520M) 1: 'ckref' falling edge (e.g. data without OSD coming from STi3520M)
Bits 3-1	del	Luma Path Delay, del[2-0]. Delay on luma path with reference to chroma path (see Table 16-6).
Bit 0	Rsv	Reserved. This bit reads as '0'.

Table 16-6. Luma Path Delay

Bit 3 del2	Bit 2 del1	Bit 1 del0	Delay on luma path with reference to chroma path
			One pixel corresponds to 1/13.5 MHz (74.04 ns)
0	0	0	+ 2 pixel delay on luma
0	0	1	+ 1 pixel delay on luma
0	1	0	+ 0 pixel delay on luma
0	1	1	- 1 pixel delay on luma
1	0	0	- 2 pixel delay on luma
Other			+ 0 pixel delay on luma

TV OUTPUT PORT

16.6.5. REGISTER_4 - CONFIGURATION 4

Config_4

Access = 84CA000h

Regoffset = 004h

7	6	5	4	3	2	1	0
syncin_ad1	syncin_ad0	syncout_ad1	syncout_ad0	aline	del_42	del_41	del_40
Default value after reset = 00000000h							

Bit Number	Mnemonic	Description
Bits 7-6	syncin_ad	Adjustment of incoming sync signals, syncin_ad[1-0]. Used to insure correct interpretation of incoming video samples as Y, Cr or Cb when the encoder is slaved to incoming sync signals (incl. 'F/H' flags stripped off ITU-R656/D1 data) (see Table 16-7).
Bits 5-4	syncout_ad	Adjustment of outgoing sync signals, syncout_ad[1-0]. Used to insure correct interpretation of incoming video samples as Y, Cr or Cb when the encoder is master and supplies sync signals (see Table 16-8).
Bit 3	aline	Video active line duration control, aline. 0: Full digital video line encoding (720 pixels - 1440 clock cycles) 1: Active line duration follows ITU-R/SMPTE 'analog' standard requirements
Bits 2-0	del_4	Luma Path Delay del4[2-0]: delay on luma path with reference to chroma path on YUV and RGB outputs when 4:4:4 input is used (see Table 16-9).

Table 16-7. Incoming Sync Adjustment

Bit 7 syncin_ad1	Bit 6 syncin_ad0	Internal delay undergone by incoming sync
0	0	Nominal
0	1	+1 ckref
1	0	+2 ckref
1	1	+3 ckref

Table 16-8. Outgoing Sync Adjustment

Bit 5 syncout_ad1	Bit 4 syncout_ad0	Delay added to sync signals before they are output
0	0	Nominal
0	1	+1 ckref
1	0	+2 ckref
1	1	+3 ckref

Table 16-9. Luma Path Delay

Bit 2	Bit 1	Bit 0	Delay on luma path with reference to chroma path in 4:4:4 encodings [One pixel corresponds to $2/f_{denc_ref_ck}$]
0	1	0	+ 2 pixel delay on luma
0	0	1	+ 1 pixel delay on lum
0	0	0	+ 0 pixel delay on luma
1	1	1	- 1 pixel delay on luma
1	1	0	- 2 pixel delay on luma
Other			+ 0 pixel delay on luma

TV OUTPUT PORT

16.6.6. REGISTER_5 - CONFIGURATION 5

Config_5

Access = 84CA000h

Regoffset = 005h

7	6	5	4	3	2	1	0
selrst_inc	bkdac1	bkdac2	bkdac3	bkdac4	bkdac5	bkdac6	dacinv
Default value after reset = 0X00h							

Bit Number	Mnemonic	Description
Bit 7	selrst_inc	Select Reset Increment, selrst_inc : Choice of Digital Frequency Synthesiser increment after soft reset or when ph_rst_mode = '01'(see Register 8) 0: Hard wired value (depending on TV standard) 1: Soft (value from registers 10 to 12)
Bit 6	bkdac1	Blanking of DACs, bkdacN. (N= 1,2,3,4,5,or 6) 0: DAC N in normal operation 1: DAC N input code forced to black level (If RGB, UV or C) or blanking level (If Y or CVBS) depending on conf_out bits of REGISTER_8 CONFIGURATION8
Bit 5	bkdac2	
Bit 4	bkdac3	
Bit 3	bkdac4	
Bit 2	bkdac5	
Bit 1	bkdac6	
Bit 0	dacinv	DAC Code Invert, dacinv. 'Inverts' DAC codes to compensate for an inverting output stage in the application. 0: DAC non inverted inputs 1: DAC inverted inputs

16.6.7. REGISTER_6 - CONFIGURATION6

Config_6

Access = 84CA000h

Regoffset = 006h

7	6	5	4	3	2	1	0
softreset	jump	dec_ninc	free_jump	cfc1	cfc0	Rsv	maxdyn
Default value after reset =010h							

Bit Number	Mnemonic	Description
Bit 7	softreset	Software reset, softreset. 0: No reset 1: Software reset Note: Bit 'softreset' is automatically reset after internal reset generation. Software reset is active during 4 CKREF periods. When softreset is activated,, all the device is reset as with hardware reset except for the first six user registers (configurations) and for registers 10 up to 14 (increment and phase of oscillator), 31-33, 34-37 and 39-42.
Bit 6	jump	jump (see Table 16-10). Note: bit "jump" is automatically reset after use.
Bit 5	dec_ninc	dec_ninc (see Table 16-10). Note: bit "jump" is automatically reset after use.
Bit 4	free_jump	free_jump (see Table 16-10). Note: bit "jump" is automatically reset after use.
Bits 3-2	cfc	MColour frequency control via CFC line, cfc[1-0] (see Table 16-11).
Bit 1	Rsv	Reserved. This bit read as '0'.
Bit 0	maxdyn	Max dynamic magnitude allowed on YCrCb inputs for encoding, max-dyn. 0: 10h to EBh for Y, 10h to E0h for chrominance (Cr,Cb) 1: 01h to FEh for Y, Cr and Cb Note: In any case, EAV and SAV words are replaced by blanking values before being fed to the luminance and chrominance processing,

TV OUTPUT PORT

Table 16-10. Line Mode

Bit 6	Bit 5	Bit 4	Description
jump	dec_ninc	free_jump	Line Mode
0	0	0	Normal mode (no line skip/insert capability) CCIR : 313/312 or 263/262 non-interlaced : 312/312 or 262/262
0	x	1	Manual mode for line insert ("dec_ninc" = '0') or skip ("dec_ninc" = '1') capability. Both fields of all the frames following the writing are modified according to "lref" and "ltarg" bits of registers 21-22-23 (by default, "lref" = '0' and "ltarg" = '1' which leads to normal mode above).
1	0	0	Automatic line insert mode. The 2 nd field of the frame following the writing is increased. Line insertion is done after line 245 in 525/60 and after line 330 in 625/50. "lref" and "ltarg" bits are ignored.
1	1	0	Automatic line skip mode. The 2 nd field of the frame following the writing is decreased. Line suppression is done after line 245 in 525/60 and after line 330 in 625/50. "lref" and "ltarg" bits are ignored.
1	x	1	Not be used

Table 16-11. MColour Frequency Control

Bit 3	Bit 2	MColour frequency Control
0	0	Disable (update done by loading of registers 10,11 and 12).
0	1	Update of increment for DDFS just after serial loading via CFC
1	0	Update of increment for DDFS on next active edge of HSYNC.
1	1	Update of increment for DDFS just before next colour burst.

16.6.8. REGISTER_7

Reserved.

16.6.9. REGISTER_8 CONFIGURATION8

Config_8

Access = 84CA000h

Regoffset = 008h

7	6	5	4	3	2	1	0
ph_rst_mode 1	ph_rst_mode 0	conf_out1	conf_out0	blk_all	Rsv	Rsv	Rsv
Default value after reset =020h							

Bit Number	Mnemonic	Description
Bits 7-6	ph_rst_mode[1-0]	Sub-carrier phase reset mode, ph_rst_mode[1-0] (see Table 16-12).
Bits 5-4	conf_out[1-0]	DENC output configuration, conf_out[1-0] (see Table 16-13).
Bit 3	blk_all	Blanking of all video lines, blk_all 0: Disabled 1: Enabled (all inputs are ignored - 80h instead of Cr and Cb and 10h instead of Y and Y4)
Bits 2-0	Rsv	Reserved

Table 16-12. Sub-carrier Phase Reset Mode

Bit 7	Bit 6	ph_rst_mode[1-0]
0	0	disabled
0	1	enabled - phase is updated with value from phase buffer register (see Reg2 bit rstosc_buf) on the beginning of the next video line. In the same time increment is updated with hard or soft value depending on selreg_inc value (see Register 5)
1	0	enabled - phase is updated with value from Registers 10 and 11 on the next increment updating by cfc (depending on cfc loading moment and Register6 cfc(1:0) bits.
1	1	enabled - phase is reset after detecting of rst bit on cfc line, up to 9 denc_ref_ck after loading of cfc's LSB. (see next figure)
Note: Bits 'ph_rst_mode(1:0)' are automatically set back to '00' after the oscillator reset has been performed in modes '01' and '10'.		

TV OUTPUT PORT

Table 16-13. Denc Output Configuration

Bit 5	Bit 4	dac1	dac2	dac3	dac4	dac5	dac6
0	0	Y	C	CVBS	C	Y	CVBS
0	1	Y	C	CVBS	V	Y	U
*1	x	Y	C	CVBS	R	G	B
Note: If set_4:4:4 = '1' (Reg2) and conf_out(1:0) = '01' then dac5 output Y coming from Y4 input.							

16.6.10. REGISTER_9 - STATUS (READ ONLY)

Stat_9

Access = 84CA000h

Regoffset = 009h

7	6	5	4	3	2	1	0
hok	atfr	buf2_free	buf1_free	fieldct2	fieldct1	fieldct0	jumping
Default value after reset = 00000000h							

Bit Number	Mnemonic	Description
Bit 7	hok	Hamming OK, hok. 0: Consecutive errors 1: A single or no error Note: signal quality detector is issued from Hamming decoding of EAV, SAV from YCrCb.
Bit 6	atfr	Frame synchronization flag, atfr. (slave mode only) 0: Encoder not synchronised 1: Encoder synchronised
Bit 5	buf2_free	Closed caption registers access condition for field 2, buf2_free. Closed caption data for field 2 is buffered before being output on the relevant TV line; buf2_free is reset if the buffer is temporarily unavailable. If the micro-controller can guarantee that registers 41 and 42 (cccf2) are never written more than once between two frame reference signals,, then bit 'buf2_free' will always be true (set). Otherwise,, closed caption field2 registers access might be temporarily forbidden by resetting bit 'buf2_free' until the next field2 closed caption line occurs. Note that this bit is false (reset) when 2 pairs of data bytes are awaiting to be encoded,, and is set back immediately after one of these pairs has been encoded (so at that time, encoding of the last pair of bytes is still pending) Reset value = '1' (access authorised)
Bit 4	buf1_free	Closed caption registers access condition for field 1, buf1_free. Same as buf2_free but concerns field 1. Reset value = '1' (access authorised)
Bits 3-1	fieldct	Digital field identification number, fieldct[2-0]. (See Table 16-14) fieldct[0] also represents the odd/even information (odd='0', even='1') .
Bit 0	jumping	Frame Jumping. This bit indicates whether a frame length modification has been programmed at '1' from programming of bit 'jump' to end of frame(s) concerned. Refer to register 6 (Section 16.6.7.) and registers 21-22-23 (Section 16.6.19.).

Table 16-14. Digital Field Identification Number

Bit 3	Bit 2	Bit 1	Digital Field Identification Number
0	0	0	Indicates field 1
...
1	1	1	Indicates field 8

TV OUTPUT PORT

16.6.11. REGISTER_10.INCREMENT_DFS REGISTER_11.INCREMENT_DFS REGISTER_12.INCREMENT_DFS

Increment for digital frequency synthesiser. These registers contain the 24-bit increment used by the DDFS if bit 'selrst' equals '1' to generate the frequency of the subcarrier i.e. the address that is supplied to the sine ROM. It therefore allows customization of the subcarrier frequency synthesiser.

<i>incr_10</i>				Access = 84CA000h				Regoffset = 0Ah			
7	6	5	4	3	2	1	0				
d23	d22	d21	d20	d19	d18	d17	d16				

<i>incr_11</i>				Access = 84CA000h				Regoffset = 0Bh			
7	6	5	4	3	2	1	0				
d15	d14	d13	d12	d11	d10	d9	d8				

<i>incr_12</i>				Access = 84CA000h				Regoffset = 0Ch			
7	6	5	4	3	2	1	0				
d7	d6	d5	d4	d3	d2	d1	d0				

Programming notes:

1 LSB ~ 1.6 Hz

The procedure to validate usage of these registers instead of the hardwired values is the following:

Load the registers with the required value

Set bit 'selrst' to 1 (Reg 2)

Perform a software reset (Reg 6)

Note: The values loaded in Reg10-11-12 are taken into account after a software reset, and ONLY IF bit 'selrst' = '1' (Reg. 2).

These registers are never reset and must be explicitly written into to contain sensible information.

On hardware reset (\Rightarrow 'selrst'=0) or on soft reset with selrst='0', the DDFS is initialised with a hardwired increment, independent of Registers 10-12. These hardwired values, being out of any user register, cannot be read out of the TV Output Port. These values are:

Value d[23:0]	Frequency Synthesised f	Ref. Clock
21F07Ch for NTSC M	3.5795452 MHz	27 MHz
2A098Bh for PAL BGHIN	4.43361875 MHz	27 MHz
21F694h for PAL N	3.5820558 MHz	27 MHz
21E6F0h for PAL M	3.57561149 MHz	27 MHz

'NTSC-4.43' can be obtained with d[23:0] value, similar to PAL BGHI but with standard fixed as NTSC.

16.6.12. REGISTER_13.PHASE_DFS,
REGISTER_14.PHASE_DFS,

Static phase offset for digital frequency synthesiser (10-bit only)

Phase_13				Access = 84CA000h			Regoffset = 0Dh
7	6	5	4	3	2	1	0
-	-	-	-	-	-	o23	o22

Phase_14				Access = 84CA000h			Regoffset = 0Eh
7	6	5	4	3	2	1	0
o21	o20	o19	o18	o17	o16	o15	o14

Programming notes:

Under certain circumstances (detailed below), these registers contain the 10 MSBs of the value with which the phase accumulator of the DDFS is initialised after a 0-to-1 transition of bit 'rstosc' (Reg 2), or after a standard change, or when cyclic phase readjustment has been programmed (see bits valrst[1:0] of Reg 2). The 14 remaining LSBs loaded into the accumulator in these cases are all '0's (this allows phase reset value to be defined the with an accuracy of 0.35°).

The procedure to validate usage of these registers instead of the hardwired values is as follows:

Load the registers with the required value

Set bit 'selrst' to 1 (Reg 2)

Perform a software reset (Reg 6)

Note: Registers 13-14 are never reset and must be explicitly written into to contain sensible information. If bit 'selrst'=0 (e.g. after a hardware reset), the phase offset used to reinitialise the DDFS is the hardwired value. As the hardwired values are not in a register, they cannot be read from the TV Output Port.

These are:

D9C000h for PAL BDGHI,, N,, M

1FC000h for NTSC-M

TV OUTPUT PORT

16.6.13. REGISTER_15

Reserved.

16.6.14. REGISTER_16

Reserved.

16.6.15. REGISTER_17

Reserved.

16.6.16. REGISTER_18

Reserved.

16.6.17. REGISTER_19

Reserved.

16.6.18. REGISTER_20

Reserved.

16.6.19. REGISTER_21: LINE_REG = LTARG[8:0]
REGISTER_22: LINE_REG = LTARG[0] AND LREF[8:2]
REGISTER_23: LINE_REG = LTARG[1:0]

These registers may be used to jump from a reference line (end of that line) to the beginning of a target line of the SAME FIELD.

However, not all lines can be skipped or repeated with no problem and, if needed, this functionality has to BE USED WITH CAUTION.

Reg_21 Access = 84CA000h Regoffset = 015h

7	6	5	4	3	2	1	0
ltarg8	ltarg7	ltarg6	ltarg5	ltarg4	ltarg3	ltarg2	ltarg1

Reg_22 Access = 84CA000h Regoffset = 016h

7	6	5	4	3	2	1	0
ltarg0	lref8	lref7	lref6	lref5	lref4	lref3	lref2

Reg_23 Access = 84CA000h Regoffset = 017h

7	6	5	4	3	2	1	0
lref1	lref0	-	-	-	-	-	-

Programming notes:

lref[8:0] contains in binary format the reference line from which a jump is required. ltarg[8:0] contains the target line binary number.

Default values: lref[8:0] = 000000000 and ltarg[8:0] = 000000001.

TV OUTPUT PORT

16.6.20. REGISTER_31.CGMS_BIT[1:4]
REGISTER_32.CGMS_BIT[5:12]
REGISTER_33.CGMS_BIT[13:20]

These three registers are CGMS data registers (20-bit only).

Reg_31				Access = 84CA000h				Regoffset = 01Fh	
7	6	5	4	3	2	1	0		
-	-	-	-	b1	b2	b3	b4		

Reg_32				Access = 84CA000h				Regoffset = 020h	
7	6	5	4	3	2	1	0		
b5	b6	b7	b8	b9	b10	b11	b12		

Reg_33				Access = 84CA000h				Regoffset = 021h	
7	6	5	4	3	2	1	0		
b13	b14	b15	b16	b17	b18	b19	b20		

These registers are never reset.

Word0A ⇒ bit 1....bit 3

Word0B ⇒ bit 4....bit 6

Word1 ⇒ bit 7....bit 10

Word2 ⇒ bit 11....bit 14

CRC ⇒ bit 15...bit 20 (not internally computed)

16.6.21. REGISTER_34

Reserved.

16.6.22. REGISTER_35

Reserved.

16.6.23. REGISTER_36

Reserved.

16.6.24. REGISTER_37

Reserved.

16.6.25. REGISTER_38

Reserved.

16.6.26. REGISTER_39-40 - CCCF1 :

Closed caption characters/extended data for field 1

Reg_39

Access = 84CA000h

Regoffset = 027h

7	6	5	4	3	2	1	0
opc11	c117	c116	c115	c114	c113	c112	c111

Bit Number	Mnemonic	Description
Bit 7	opc11	Odd-parity bit of US-ASCII 7-bit character c11[7:1], opc11. First byte to encode in field1.

Reg_40

Access = 84CA000h

Regoffset = 028h

7	6	5	4	3	2	1	0
op12	c127	c126	c125	c124	c123	c122	c121

Bit Number	Mnemonic	Description
Bit 7	op12	Odd-parity bit of US-ASCII 7-bit character c12[7:1], opc12. Second byte to encode in field1.

Programming notes:

Default value: none, but closed caption enabling without loading these registers will issue character NULL.

Registers 39-40 are never reset.

TV OUTPUT PORT

16.6.27. REGISTER_41.CCCF2 REGISTER_42.CCCF2

Closed caption characters/extended data for field 2.

Reg_41

Access = 84CA000h

Regoffset = 029h

7	6	5	4	3	2	1	0
opc21	c217	c216	c215	c214	c213	c212	c211

Bit Number	Mnemonic	Description
Bit 7	opc21	Odd-parity bit of US-ASCII 7-bit character c21[7:1], opc11. First byte to encode in field2.

Reg_42

Access = 84CA000h

Regoffset = 02Ah

7	6	5	4	3	2	1	0
op22	c227	c226	c225	c224	c223	c222	c221

Bit Number	Mnemonic	Description
Bit 7	op22	Odd-parity bit of US-ASCII 7-bit character c22[7:1], opc12. Second byte to encode in field2.

Programming notes:

Default value: none but closed captions enabling without loading these registers will issue character NULL.

Registers 41-42 are never reset.

16.6.28. REGISTER_43 - CCLIF1

Closed caption/extended data line insertion for field 1.

TV line number where closed caption/extended data is to be encoded in field 1 is programmable through the following register:

Reg_43		Access = 84CA000h				Regoffset = 02Bh	
7	6	5	4	3	2	1	0
-	-	-	I1_4	I1_3	I1_2	I1_1	I1_0

MSB				LSB				
register_43	x	x	x	I1_4	I1_3	I1_2	I1_1	I1_0

Programming notes:

525/60 system: (525-SMPTE line number convention)

Only lines 10 through 22 should be used for closed caption or extended data services (line 1 through 9 contain the vertical sync pulses with equalizing pulses).

I1[4:0] = 00000 no line selected for closed caption encoding

I1[4:0] = 000xx do not use these codes

...

I1[4:0] = i code line (i+6) (SMPTE) selected for encoding

...

I1[4:0] = 11111 line 37 (SMPTE) selected

625/50 system: (625-CCIR/ITU-R line number convention)

Only lines 7 through 23 should be used for closed caption or extended data services.

I1[4:0] = 00000 no line selected for closed caption encoding

...

I1[4:0] = i code line (i+6) (CCIR) selected for encoding (i > 0)

...

I1[4:0] = 11111 line 37 (CCIR) selected

(*) Default value = 01111 line 21 (525/60, 525-SMPTE line number convention). This value also corresponds to line 21 in 625/50 system, (625-CCIR line number convention).

17. LOCAL BUS INTERFACE

17.1. INTRODUCTION

The Local Bus interface of the STPC provides a low latency bus to external peripheral cards at HCLK. The Local Bus may operate in asynchronous or synchronous modes through the 22-bit address and 16-bit data bus.

The Local Bus interface supports up to two memory devices and four I/O devices. It can support up to 32 MBytes of memory for each of the memory chip selects and from 4 Byte to 1 KByte of I/O space for each of the I/O devices. All the chip select timings are individually programmable. This interface can be accessed only by the CPU.

The memory addresses are predefined for the memory chip selects. The first bank of the memory is intended to be used as a boot device.

The starting address for each IO chip select is programmable at 4 Byte boundary. The access range for each of the chip select is also programmable. The size varies from 4 Bytes to 1 KByte.

17.2. LOCAL BUS REGISTERS

The Local Bus configuration registers can be categorised into three groups:

1. Address Decode Registers,
2. Timing Registers,
3. Control Register.

All registers, except the CONTROL and IOWIDTH Register, are 16-bit wide. These registers are accessible only by the CPU. All registers are accessed through I/O Port 22h and Port 23h. Port 22h is used as the index to the register bank and Port 23h is used as the data port. This way, the CPU can access only 8 bits of register data at a time, so two accesses are required to completely read or write the 16-bit registers. The lower and upper halves of the 16-bit registers have the same index values. First access after reset with the given index will map to the lower Byte of the register. The next access with the same index will access the upper Byte. For the 8-bit registers (CONTROL Register Index 1Ch and IOWIDTH Register Index 1Eh) data must be written and read twice as they are seen as 16-bit registers. [Table 17-1.](#) below shows Local Bus Register Indices.

Table 17-1. Local Bus Register Indices

Name	Index	Function
IOAREG0	10h	Address Decode
IOAREG1	11h	
IOAREG2	12h	
IOAREG3	13h	
IOMREG0 (Slot 0 & 1)	14h	
IOMREG1 (Slot 2 & 3)	15h	
TIMEBANK0	16h	Timing
TIMEBANK1	17h	
TIMEIO0	18h	
TIMEIO1	19h	
TIMEIO2	1Ah	
TIMEIO3	1Bh	
CONTROL	1Ch	Control
IOWIDTH	1Eh	

There are two other ways in which these registers can be accessed. These approaches are described in the Control Register [Section 17.5.1.](#)

LOCAL BUS INTERFACE

17.3. LOCAL BUS ADDRESS DECODE REGISTERS

17.3.1. I/O SLOT BASE ADDRESS REGISTER 0

This 16-bit register defines the starting address (4 Bytes or 32-bit DWORD) and I/O address spaces mapped on the Local Bus. The base address for I/O slot 0 is specified in register IOAREG0. Any accesses that hit onto the address range defined by this register and its mask (in the corresponding low Byte of the IOMREG0 register) asserts the IOCS0# and will prevent the cycle being forwarded onto the PCI bus.

IOAREG0

Access = 0022h/0023h

Regoffset = 10h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SA														Rsv	
Default value after reset = 0FFh															

Bit Number	Mnemonic	Description
Bits 15-2	SA	Starting Address aligned to 4 I/O locations.
Bits 1-0	Rsv	Reserved.

Programming notes:

The two memory address spaces (for Memory Devices devices) have a fixed range:

- FF000000h - FFFFFFFFh for the Boot device
- FE000000h - FFFFFFFFh for the second device.

17.3.2. I/O SLOT BASE ADDRESS REGISTER 1

This 16-bit register defines the starting address (4 Bytes or 32-bit DWORD) and I/O address spaces mapped on the Local Bus. The base address for I/O slot 1 is specified in register IOAREG1. Any accesses that hit onto the address range defined by this register and its mask (in the corresponding high Byte of the IOMREG0 register) asserts the IOCS1# and will prevent the cycle being forwarded onto the PCI bus.

IOAREG1

Access = 0022h/0023h

Regoffset = 11h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SA														Rsv	
Default value after reset = 0FFh															

Bit Number	Mnemonic	Description
Bits 15-2	SA	Starting Address aligned to 4 I/O locations.
Bits 1-0	Rsv	Reserved.

LOCAL BUS INTERFACE

17.3.3. I/O SLOT BASE ADDRESS REGISTER 2

This 16-bit register defines the starting address (4 Bytes or 32-bit DWORD) and I/O address spaces mapped on the Local Bus. The base address for I/O slot 2 is specified in register IOAREG2. Any accesses that hit onto the address range defined by this register and its mask (in the corresponding low Byte of the IOMREG1 register) asserts the IOCS2# and will prevent the cycle being forwarded onto the PCI bus.

IOAREG2

Access = 0022h/0023h

Regoffset = 12h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SA														Rsv	
Default value after reset = 0FFh															

Bit Number	Mnemonic	Description
Bits 15-2	SA	Starting Address aligned to 4 I/O locations.
Bits 1-0	Rsv	Reserved.

17.3.4. I/O SLOT BASE ADDRESS REGISTER 3

This 16-bit register defines the starting address (4 Bytes or 32-bit DWORD) and I/O address spaces mapped on the Local Bus. The base address for I/O slot 3 is specified in register IOAREG3. Any accesses that hit onto the address range defined by this register and its mask (in the corresponding high Byte of the IOMREG1 register) asserts the IOCS3# and will prevent the cycle being forwarded onto the PCI bus.

IOAREG3

Access = 0022h/0023h

Regoffset = 13h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SA														Rsv	
Default value after reset = 0FFh															

Bit Number	Mnemonic	Description
Bits 15-2	SA	Starting Address aligned to 4 I/O locations.
Bits 1-0	Rsv	Reserved.

LOCAL BUS INTERFACE

17.3.5. I/O SLOT MASK REGISTER 0

The address mask register IOMREG0 defines the size of the two first I/O slots. The 8-bit address mask for each slot will mask the address that we do not want to compare during the address decoding process. The 8-bit mask will filter bit 9:2 of the starting address specified in the corresponding IOAREG, allowing a selection of 4, 8, 16, 32, 64, 128, 256, 512 or 1K continuous or non continuous locations.

IOMREG0

Access = 0022h/0023h

Regoffset = 14h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AMIO1								AMIO0							
Default value after reset =															

Bit Number	Mnemonic	Description
Bits 15-8	AMIO1	Address mask for I/O Slot 1.
Bits 7-0	AMIO0	Address mask for I/O Slot 0.

Table 17-2. 8 bit Address Mask

8-bit Address Mask	I/O Space Size (Bytes)
0000 0000	4
0000 0001	8
0000 0011	16
0000 0111	32
0000 1111	64
0001 1111	128
0011 1111	256
0111 1111	512
1111 1111	1024

Note: To define an address range requires that the base address be aligned to the range (i.e. a whole multiple of the width). See [Table 17-2](#).

Example; I/O Width = 32 (Mask = 07)

I/O Range = X X + 31

Then X must be an whole multiple of 32.

17.3.6. I/O SLOT MASK REGISTER 1

The address mask register IOMEREG1 defines the size of I/O slots 2 & 3. The 8-bit address mask for each slot will mask the address that we do not want to compare during the address decoding process. The 8-bit mask will filter bit 9:2 of the starting address specified in the corresponding IOAREG allowing a selection of 4, 8, 16, 32, 64, 128, 256, 512 or 1K continuous or non continuous locations.

IOMREG1

Access = 0022h/0023h

Regoffset = 15h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AMIO3								AMIO2							
Default value after reset =															

Bit Number	Mnemonic	Description
Bits 15-8		Address mask for I/O Slot 3.
Bits 7-0		Address mask for I/O Slot 2.

LOCAL BUS INTERFACE

17.4. LOCAL BUS TIMING REGISTERS

17.4.1. MEMORY TIMING TEMPLATE REGISTER 0

This register defines the timing template for accessing Memory Devices bank 0. The timing is programmed with reference to the host clock period as a time unit.

Timing for FLASH devices should take into account access times of 60ns and 150ns for the Boot Memory.

TIMEBANK0

Access = 0022h/0023h

Regoffset = 16h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSH	UARS	CHT			CAT								CST		
Default value after reset =															

Bit Number	Mnemonic	Description
Bit 15	DSH	Discard the Setup and Hold parameters for read operations.
Bit 14	UARS	Use asynchronous ready signal for command termination. The asynchronous ready enable bit sets the Local Bus logic to wait for an external ready signal before closing the current cycle.
Bits 13-11	CHT	Command Hold time , and is determined as follows: Command hold time = $(5+V_h) \times T$ Where V_h = Register value for the Hold time T = HCLK period.
Bits 10-3	CAT	Command Active time , and is determined as follows: Command active time = $(2+V_a) \times T$ Where V_a = Register value for the Active time T = HCLK period.
Bits 2-0	CST	Command Setup time , and is determined as follows: Command setup time = $(4+V_s) \times T$ Where V_s = Register value for the Setup time T = HCLK period.

17.4.2. MEMORY TIMING TEMPLATE REGISTER 1

This register defines the timing template for accessing Memory Devices bank 1. The timing is programmed with reference to the host clock period as a time unit.

Timing for FLASH devices should take into account access times of 60ns and 150ns for the Boot Memory.

TIMEBANK1

Access = 0022h/0023h

Regoffset = 17h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSH	UARS	CHT			CAT								CST		
Default value after reset =															

Bit Number	Mnemonic	Description
Bit 15	DSH	Discard the Setup and Hold parameters for read operations.
Bit 14	UARS	Use asynchronous ready signal for command termination. The asynchronous ready enable bit sets the Local Bus logic to wait for an external ready signal before closing the current cycle.
Bits 13-11	CHT	Command Hold time , and is determined as follows: Command hold time = $(5+V_h) \times T$ Where V_h = Register value for the Hold time T = HCLK period.
Bits 10-3	CAT	Command Active time , and is determined as follows: Command active time = $(2+V_a) \times T$ Where V_a = Register value for the Active time T = HCLK period.
Bits 2-0	CST	Command Setup time , and is determined as follows: Command setup time = $(4+V_s) \times T$ Where V_s = Register value for the Setup time T = HCLK period.

LOCAL BUS INTERFACE

17.4.3. I/O TIMING TEMPLATE REGISTER 0

This register defines the timing template for accessing device in I/O Slot 0. The timing is programmed with reference to the host clock period as a time unit.

TIMEIO0

Access = 0022h/0023h

Regoffset = 18h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSH	UARS	CHT			CAT								CST		
Default value after reset =															

Bit Number	Mnemonic	Description
Bit 15	DSH	Discard the Setup and Hold parameters for read operations.
Bit 14	UARS	Use asynchronous ready signal for command termination. The asynchronous ready enable bit sets the Local Bus logic to wait for an external ready signal before closing the current cycle.
Bits 13-11	CHT	Command Hold time , and is determined as follows: Command hold time = $(8+V_h) \times T$ Where V_h = Register value for the Hold time T = HCLK period.
Bits 10-3	CAT	Command Active time , and is determined as follows: Command active time = $(3+V_a) \times T$ Where V_a = Register value for the Active time T = HCLK period.
Bits 2-0	CST	Command Setup time , and is determined as follows: Command setup time = $(4+V_s) \times T$ Where V_s = Register value for the Setup time T = HCLK period.

17.4.4. I/O TIMING TEMPLATE REGISTER 1

This register defines the timing template for accessing device in I/O Slot 1. The timing is programmed with reference to the host clock period as a time unit.

TIMEIO1

Access = 0022h/0023h

Regoffset = 19h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSH	UARS	CHT			CAT								CST		
Default value after reset =															

Bit Number	Mnemonic	Description
Bit 15	DSH	Discard the Setup and Hold parameters for read operations.
Bit 14	UARS	Use asynchronous ready signal for command termination. The asynchronous ready enable bit sets the Local Bus logic to wait for an external ready signal before closing the current cycle.
Bits 13-11	CHT	Command Hold time , and is determined as follows: Command hold time = $(8+V_h) \times T$ Where V_h = Register value for the Hold time T = HCLK period.
Bits 10-3	CAT	Command Active time , and is determined as follows: Command active time = $(8+V_a) \times T$ Where V_a = Register value for the Active time T = HCLK period.
Bits 2-0	CST	Command Setup time , and is determined as follows: Command setup time = $(4+V_s) \times T$ Where V_s = Register value for the Setup time T = HCLK period.

LOCAL BUS INTERFACE

17.4.5. I/O TIMING TEMPLATE REGISTER 2

This register defines the timing template for accessing device in I/O Slot 2. The timing is programmed with reference to the host clock period as a time unit.

TIMEIO2

Access = 0022h/0023h

Regoffset = 1Ah

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSH	UARS	CHT			CAT								CST		
Default value after reset =															

Bit Number	Mnemonic	Description
Bit 15	DSH	Discard the Setup and Hold parameters for read operations.
Bit 14	UARS	Use asynchronous ready signal for command termination. The asynchronous ready enable bit sets the Local Bus logic to wait for an external ready signal before closing the current cycle.
Bits 13-11	CHT	Command Hold time , and is determined as follows: Command hold time = $(8+V_h) \times T$ Where V_h = Register value for the Hold time T = HCLK period.
Bits 10-3	CAT	Command Active time , and is determined as follows: Command active time = $(3+V_a) \times T$ Where V_a = Register value for the Active time T = HCLK period.
Bits 2-0	CST	Command Setup time , and is determined as follows: Command setup time = $(4+V_s) \times T$ Where V_s = Register value for the Setup time T = HCLK period.

17.4.6. I/O TIMING TEMPLATE REGISTER 3

This registers defines the timing template for accessing device in I/O Slot 3. The timing is programmed with reference to the host clock period as a time unit.

TIMEIO3

Access = 0022h/0023h

Regoffset = 1Bh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSH	UARS	CHT			CAT								CST		
Default value after reset =															

Bit Number	Mnemonic	Description
Bit 15	DSH	Discard the Setup and Hold parameters for read operations.
Bit 14	UARS	Use asynchronous ready signal for command termination. The asynchronous ready enable bit sets the Local Bus logic to wait for an external ready signal before closing the current cycle.
Bits 13-11	CHT	Command Hold time , and is determined as follows: Command hold time = $(8+V_h) \times T$ Where V_h = Register value for the Hold time T = HCLK period.
Bits 10-3	CAT	Command Active time , and is determined as follows: Command active time = $(3+V_a) \times T$ Where V_a = Register value for the Active time T = HCLK period.
Bits 2-0	CST	Command Setup time , and is determined as follows: Command setup time = $(4+V_s) \times T$ Where V_s = Register value for the Setup time T = HCLK period.

LOCAL BUS INTERFACE

17.5. LOCAL BUS CONTROL REGISTER

17.5.1. CONTROL REGISTER

CONTROL

Access = 0022h/0023h

Regoffset = 1Ch

7	6	5	4	3	2	1	0
RAM		32AFME	CEB1	CEB0	WEB1	WEB0	RMBAE
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-6	RAM	Register Access Map. See Table 17-3 .
Bit 5	32AFME	32 bit access to Memory Devices Enable. Setting this bit enables 32-bit access to both bank1 and bank0.
Bit 4	CEB1	Cache Enable for Bank1.
Bit 3	CEB0	Cache Enable for Bank0.
Bit 2	WEB1	Write Enable for Bank1.
Bit 1	WEB0	Write Enable for Bank0.
Bit 0	RMBAE	Real Mode Boot Access Enable. When set this bit enables boot access in Real Mode by mapping 000C0000h to FFFC0000h and 000FFFFFh to FFFFFFFFh.

Table 17-3. Register Access Map

Bit 7	Bit 6	Register Access
0	0	Access with same index will alternately map to lower and upper and lower Bytes of the 16 bit register as described in Section 17.2 .
0	1	Register accesses will always map to the lower Byte.
1	0	Register accesses will always map to the upper Byte.
1	1	Access with same index will alternately map to lower and upper and lower Bytes of the 16 bit register as described in Section 17.2 .

17.5.2. IO WIDTH REGISTER

This is an 8-bit register where the four less significant bits are used to tell the local bus if an 8-bit or 16-bit peripheral is attached to one of the four I/O slots.

IOWIDTH

Access = 0022h/0023h

Regoffset = 1Eh

7	6	5	4	3	2	1	0
Rsv				IOW3	IOW2	IOW1	IOW0
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-4	Rsv	Reserved.
Bit 3	IOW3	If set to 1, the I/O 3 is a 16 bit peripheral, if set to 0 it is an 8 bit peripheral.
Bit 2	IOW2	If set to 1, the I/O 2 is a 16 bit peripheral, if set to 0 it is an 8 bit peripheral.
Bit 1	IOW1	If set to 1, the I/O 1 is a 16 bit peripheral, if set to 0 it is an 8 bit peripheral.
Bit 0	IOW0	If set to 1, the I/O 0 is a 16 bit peripheral, if set to 0 it is an 8 bit peripheral.

LOCAL BUS INTERFACE

17.6. CHIP SELECT MEMORY MAP

The address mapping supported by the Local Bus interface is summarised in [Table 17-4](#). Memory address ranges are mapped at fixed addresses while the I/O devices can be mapped from 1 DWord (double word) to 256 DWord inside a 16-MByte segment.

Table 17-4. Local Bus Address Mapping

Memory Devices Chip Select	Bank 0		Bank 1	
Address Range	FF000000h-FFFFFFFFh		FE000000h-FEFFFFFFh	
Address Space	16 MBytes		16 MBytes	
Boot Address Space (Real Mode)	000C0000h-000FFFFFFH		-	
I/O Control Chip Select	IOCS#0	IOCS#1	IOCS#2	IOCS#3
Address Range	0000h-FFFFh	0000h-FFFFh	0000h-FFFFh	0000h-FFFFh
Address Space	4 Bytes - 1KByte	4 Bytes - 1KByte	4 Bytes - 1KByte	4 Bytes - 1KByte

Memory access to the Local Bus is based on the following logic scheme, see [Figure 17-1](#).

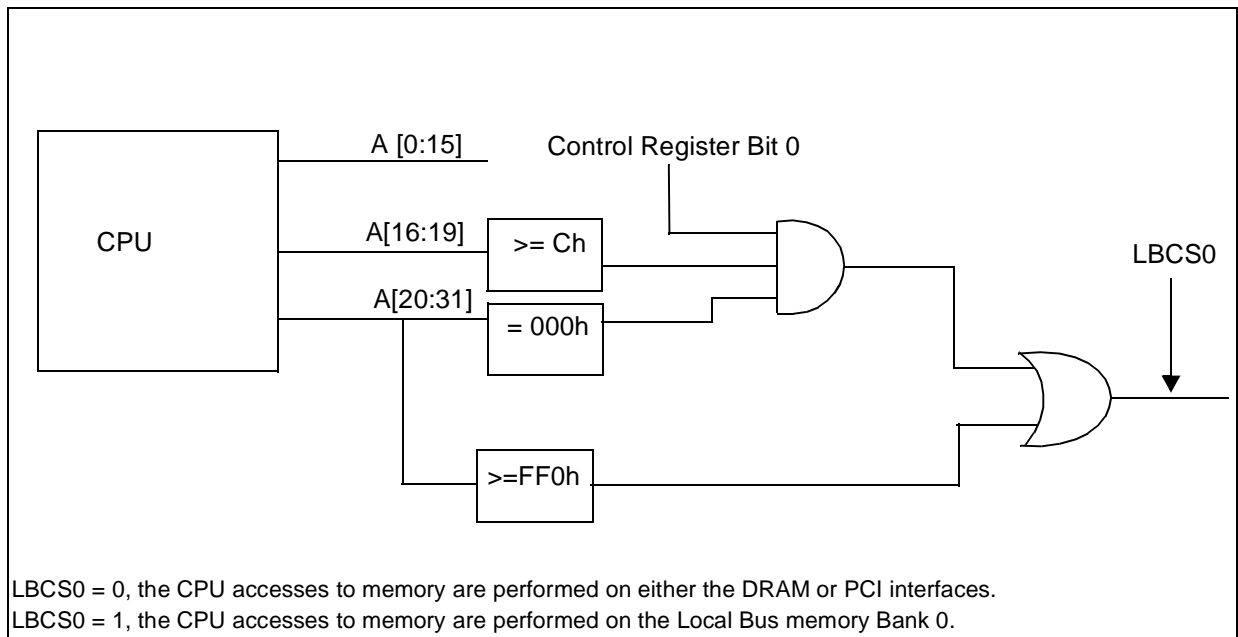


Figure 17-1. Memory Bank 0 Access Logic

18. POWER MANAGEMENT

18.1. INTRODUCTION

For full information on the action of the System Management Mode (SMM), please refer to the STMicroelectronics manual for the ST486 CPU Core. This chapter describes the SMM control registers for the STPC.

The STPC provides the following hardware structures to assist the software in managing system power consumption:

- System Activity detection,
- Three power-down timers,
 - Doze timer for detecting short-duration lack of system activity,
 - Standby timer for detecting medium-duration lack of system activity,
 - Suspend timer for detecting long-term lack of system activity,
- House-keeping activity detection,
- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in standby state,
- Peripheral Activity detection,
- Peripheral timer for detecting lack of peripheral activity,
- STPCLK# modulation to adjust system performance in various system power down states, including full power-on state.

Lack of system activity for progressively longer periods of times is detected by the three power-down timers. These timers can generate a System Management Interrupt (SMI) to the CPU so that the SMM software can put the system in decreasing states of power consumption. System activity in a power-down state can generate an SMI to allow the software to bring the system back up to the full power-on state. The chipset supports up to three power-down states: Doze state, Standby state and Suspend state. These correspond to increasing levels of power savings.

The chipset can detect the presence or absence of the following System activities:

- DMA Request (DRQ),
- Interrupt Request (INTR),
- Parallel IO (PIO),
- Serial IO (SIO) ,
- Keyboard (KBD),
- Floppy Disk Controller (FDC),
- Hard Disk Controller (HDC) ,
- PCI master device,
- Programmable address range.

Each of these can be individually enabled. The presence of an enabled system activity resets the power-down timers. The chipset generates the SMI when no system activity is detected for the delay period programmed in the power-down timers. The software can then put the appropriate sub-systems in the power-down mode, request STPCLK# assertion and stop CPU and other system clocks, program the current power-down state in the chipset and set up the next timer.

The presence of an enabled system activity, when the STPC is in a power-down state, will first enable any stopped clocks, wait for a programmable delay to allow any internal Phase Locked Loop (PLL) to stabilise and then deassert STPCLK# to enable CPU execution. The device can optionally generate an SMI to allow the SMM to bring the system back to the power-on state.

POWER MANAGEMENT

The current revision of the STPC does not implement support for stopping CPU and other system clocks.

In Doze or Standby state, a house-keeping activity, can bring the system back to full speed for a short period of time before returning back to Doze or Standby state. The chipset can detect the following house-keeping activities:

- DMA Request (DRQ),
- Interrupt Request (INTR),
- Keyboard (KBD),
- PCI master device.

The house-keeping timer determines the length of time the system will be on before returning to the original power-down state. An activity can be either a system activity or a house-keeping activity, but not both at the same time. Further, the Suspend state cannot make use of this feature.

The absence of the following peripheral activities can be enabled to cause an SMI and thus allow the software to put the unused peripherals in the power-down state, while the remainder of the system is still in full power-on state:

- Parallel IO (PIO),
- Serial IO (SIO) ,
- Keyboard (KBD),
- Floppy Disk Controller (FDC),
- Hard Disk Controller (HDC),
- A programmable address range.

Each of these can be individually enabled for inactivity detection. The presence of a peripheral activity does not reset the peripheral timer. It always times out after the programmed delay period. An SMI is generated if any enabled peripheral was not active for this time period. The device provides IO access trapping to detect access to a powered-down peripheral, so that the software can bring the peripheral to the power-on state before the access is completed.

The STPC can also carry out software transparent power management, if so enabled. In this mode of operation, doze and standby time-outs will change the CPU clock without generating an SMI. The state transitions from fully-on to doze or standby and back to fully-on will take place automatically. Also note that the suspend state can never be entered automatically but always requires software assist.

The STPC decodes the various activities listed below in [Table 18-1](#).

Table 18-1. Activity Detected

Activity	Detected via
ISA DMA masters	Low to high transition of hold request of 206
PCI masters	High to low transition of any of PCIRQ2-0#
Parallel port	IO read/write at 378h-37Fh, 278h-27Fh and 3BCh-3BFh
Serial port	IO read/write at 3F8h-3FFh, 2F8h-2FFh, 3E8h-3EFh and 2E8h-2EFh
Keyboard	IO read/write at 60h, 62h, 64h and 66h
Floppy disk	IO read/write at 3F2h, 3F4h, 3F5h and 3F7h
Hard disk	IO read/write in 170h-177h, 376h, 1F0h-1F7h and 3F6h address range as well as any bus master activity by the internal IDE controller.

18.2. POWER MANAGEMENT CONTROLLER REGISTERS

18.2.1. TIMER REGISTER 0

This register controls the timer for the selection of the length of timeout for the doze, standby and suspend modes.

Timer0

Access = 0022h/0023h

Regoffset = 060h

7	6	5	4	3	2	1	0
SUTT			STT			Rsv	
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-5	SUTT	<p>Suspend Timeout Timer, when set to any value other than the disable value (000), this timer will generate an SMI on time out.</p> <p>Once enabled, this timer counts down from the programmed value. If any of the enabled system activities are detected before time out, the timer will reset and start again. These bits are encoded as given in Table 18-2.</p> <p>The suspend timer will count whenever it is not disabled and the suspend time-out bit in the SMI status register 0 is not set to a 1.</p>
Bits 4-2	STT	<p>Standby Timeout Timer, when set to any value other than the disable value (000) this timer, on expiration, can either generate the SMI to the CPU or if programmed for auto-power saving (software transparent power management) mode, change the power-down state to Standby state (refer to auto-power saving mode for details of the power saving features that are enabled in the standby state). Similar to the Suspend timer, presence of an enabled system activity will reset the timer to restart counting. These bits are encoded as given in Table 18-3.</p> <p>The standby timer will count whenever it is not disabled and the standby time-out bit in the SMI status register 0 is not set to a 1.</p>
Bits 1-0	Rsv	Reserved.

Table 18-2. Suspend Timer Reset

Bit 7	Bit 6	Bit 5	Suspend Timer reset
0	0	0	Disabled
0	0	1	4 minutes
0	1	0	8 minutes
0	1	1	12 minutes
1	0	0	16 minutes
1	0	1	32 minutes
1	1	0	48 minutes
1	1	1	64 minutes

Table 18-3. Standby Timer Reset

Bit 4	Bit 3	Bit 2	Standby Timer reset
0	0	0	Disabled
0	0	1	Reserved
0	1	0	2 minutes
0	1	1	4 minutes
1	0	0	6 minutes
1	0	1	8 minutes
1	1	0	12 minutes
1	1	1	16 minutes

18.2.2. TIMER REGISTER 1

Timer1

Access = 0022h/0023h

Regoffset = 061h

7	6	5	4	3	2	1	0
Rsv	HKT			PTT			Rsv
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved.
Bits 6-4	HKT	<p>House-keeping Timer. This timer determines how long the PMU will be in Doze house-keeping state when an enabled house-keeping activity is detected while in doze or standby power-down states. It is encoded as given in Table 18-4.</p> <p>The house-keeping counts only when the PMU is in one of the house-keeping states. Another house-keeping activity while the controller is in house_keeping state will reset the house-keeping timer to restart counting. A system activity detection in the house_keeping state will have the same effect as if the controller was in Doze or Standby state. Either an SMI will be generated to allow the software to bring the system to power-on state or the controller will automatically transition to power-on state. The house-keeping timer and function can be disabled by masking out all activity detection via the House-keeping Enable registers.</p>
Bits 3-1	PTT	<p>Peripheral Timeout Timer. When set to a value other than (000) this timer on expiration, will generate an SMI if any of the enabled peripherals remained inactive during the entire period. Unlike the power-down timers, the peripheral timer does not reset due to an enabled peripheral activity. It always times out after the programmed delay. An SMI is generated only if any of the enabled peripherals were inactive during this period. This field is encoded as given in Table 18-5.</p> <p>The peripheral timer counts whenever it is enabled.</p>
Bit 0	Rsv	Reserved.

Table 18-4. House-keeping Timer Reset

Bit 6	Bit 5	Bit 4	House-keeping Timer reset
0	0	0	Disabled
0	0	1	64 micro-seconds
0	1	0	128 micro-seconds
0	1	1	256 micro-seconds
1	0	0	Reserved
1	0	1	4 milli-seconds
1	1	0	16 milli-seconds
1	1	1	32 milli-seconds

Table 18-5. Peripheral Timer Reset

Bit 3	Bit 2	Bit 1	Peripheral Timer reset
0	0	0	Disabled
0	0	1	8 seconds
0	1	0	16 seconds
0	1	1	32 seconds
1	0	0	64 seconds
1	0	1	128 seconds
1	1	0	256 seconds
1	1	1	512 seconds

18.2.3. TIMER REGISTER 2

Timer 2

Access = 0022h/0023h

Regoffset = 08Dh

7	6	5	4	3	2	1	0
DTT			Rsv				
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7- 5	DTT	Doze Timeout Timer. When set to any value other than the disable value (00), this timer, on expiration, can either generate the SMI to the CPU or if programmed for auto-power saving (software transparent power management) mode, change the power-down state to Doze state (refer to auto-power saving mode for details of the power saving features that are enabled with Doze state). Similar to the suspend timer, presence of an enabled system activity will reset the timer to restart counting. This 3-bit field is encoded as given in Table 18-6 . The doze timer will count whenever it is not disabled and the doze time-out bit in the SMI status register 0 is not set to a '1'.
Bits 4-2	Rsv	Reserved.

Table 18-6. Doze Timer Reset

Bit 7	Bit 6	Bit 5	Doze Timer reset
0	0	0	Disabled
0	0	1	50 milli-seconds
0	1	0	100 milli-seconds
0	1	1	500 milli-seconds
1	0	0	Reserved
1	0	1	4 seconds
1	1	0	8 seconds
1	1	1	16 seconds

POWER MANAGEMENT

18.2.4. SYSTEM ACTIVITY ENABLE REGISTER 0

This is the first of the three registers that control which system activity to detect.

Sys_Activ_en0

Access = 0022h/0023h

Regoffset = 062h

7	6	5	4	3	2	1	0
DRQ	PCIM	PIO	SIO	KBD	FDC	HDC	Rsv
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	DRQ	DMA Request (DRQ).
Bit 6	PCIM	PCI master device (PCIM).
Bit 5	PIO	Parallel IO (PIO).
Bit 4	SIO	Serial IO (SIO).
Bit 3	KBD	Keyboard (KBD).
Bit 2	FDC	Floppy Disk Controller (FDC).
Bit 1	HDC	Hard Disk Controller (HDC).
Bit 0	Rsv	Reserved.

Programming notes:

When detected, the power-down timers will reload with their initial time values, or if enabled via the SMI control register, an SMI will be generated, or if programmed for auto-power down mode and in Doze or Standby power-down states, transition to power-on state will take place. Set the following bits to '1' to detect the associated activity, and to '0' to ignore the associated activity.

18.2.5. SYSTEM ACTIVITY ENABLE REGISTER 1

This is the second of the three registers that control which system activity to detect.

Sys_Activ_en1

Access = 0022h/0023h

Regoffset = 063h

7	6	5	4	3	2	1	0
Rsv		AR0	Rsv				
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved. Must be programmed to '0'.
Bit 5	AR0	Address range 0.
Bits 4-0	Rsv	Reserved. Must be programmed to '0'.

POWER MANAGEMENT

18.2.6. SYSTEM ACTIVITY ENABLE REGISTER 2

This is the third of the three registers that control which system activity to detect.

Sys_Activ_en2

Access = 0022h/0023h

Regoffset = 064h

7	6	5	4	3	2	1	0
IRQ15-1	IRQ0	NMI	Rsv				
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	IRQ15-1	IRQ15-1 detection enabled.
Bit 6	IRQ0	IRQ0 detection enabled.
Bit 5	NMI	NMI detection enable.
Bits 4-0	Rsv	Reserved.

18.2.7. HOUSE-KEEPING ACTIVITY ENABLE REGISTER 0

This register controls which house-keeping activity to detect. House-keeping activities are detected only in Doze and Standby states. If enabled, a house-keeping activity reverts the system back to power-on state for a short period of time, programmed in the house-keeping timer. Set the following bits to a '1' to enable activity detection and a '0' to ignore the associated activity.

HK_Activ_en0

Access = 0022h/0023h

Regoffset = 065h

7	6	5	4	3	2	1	0
DRQ	PCI MD	KBD	IRQ15-1	IRQ0	NMI	Rsv	
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	DRQ	DMA Request (DRQ) activity
Bit 6	PCI MD	PCI master device activity
Bit 5	KBD	Keyboards (KBD) activity
Bit 4	IRQ15-1	IRQ15-1 activity
Bit 3	IRQ0	IRQ0 activity
Bit 2	NMI	NMI activity
Bits 1-0	Rsv	Reserved.

POWER MANAGEMENT

18.2.8. HOUSE-KEEPING ACTIVITY ENABLE REGISTER 1

This is the second house-keeping activity detection enable register.

HK_Activ_en1

Access = 0022h/0023h

Regoffset = 066h

7	6	5	4	3	2	1	0
Rsv		AR0	Rsv				
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved. Must be programmed to '0'.
Bit 5	AR0	Address range 0.
Bits 4-0	Rsv	Reserved. Must be programmed to '0'.

18.2.9. PERIPHERAL INACTIVITY DETECTION REGISTER 0

This register controls which peripheral inactivity is enabled for generating an SMI on a peripheral time-out.

Perif_Inact0

Access = 0022h/0023h

Regoffset = 067h

7	6	5	4	3	2	1	0
PIO	SIO	KBD	FDC	HDC	ARO	Rsv	
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	PIO	Parallel IO (PIO) activity.
Bit 6	SIO	Serial IO (SIO) activity.
Bit 5	KBD	Keyboard (KBD) activity.
Bit 4	FDC	Floppy Disk Controller (FDC) activity.
Bit 3	HDC	Hard Disk Controller (HDC) activity.
Bit 2	ARO	Address range 0.
Bits 1-0	Rsv	Reserved. Must be programmed to '0'.

Programming notes:

Lack of peripheral activity for an enabled peripheral for one peripheral time-out period generates an SMI. A '1' in a bit position enables the SMI generation for the associated peripheral and a '0' disables it. Software can use the Peripheral Inactivity status register to determine which peripheral should be powered down.

POWER MANAGEMENT

18.2.10. PERIPHERAL ACTIVITY DETECTION REGISTER 0

This register controls which peripheral accesses will cause an SMI.

Perif_Act0

Access = 0022h/0023h

Regoffset = 069h

7	6	5	4	3	2	1	0
PIO	SIO	KBD	FDC	HDC	ARO	Rsv	
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	PIO	Parallel port (PIO) access
Bit 6	SIO	Serial port (SIO) access
Bit 5	KBD	Keyboard (KBD) access
Bit 4	FDC	Floppy Disk Controller (FDC) access
Bit 3	HDC	Hard Disk Controller (HDC) access
Bit 2	ARO	Address range 0
Bits 1-0	Rsv	Reserved. Must be programmed to '0'

Programming notes:

Typically the power management software will detect non-usage of a peripheral device via Peripheral in-activity status registers, bring the peripheral into power down state and then enable trapping access to that peripheral via this register.

Thus when an application attempts to make use of a powered down peripheral, the access is trapped and an SMI is generated to allow software to re-power the peripheral device before allowing the access to complete. This register is the first of the two such registers.

A '1' in a bit position enables SMI generation for the associate peripheral and a '0' disables.

18.2.11. PERIPHERAL ACTIVITY DETECTION REGISTER 1

This is the second register that controls which peripheral accesses will cause an SMI. This register is similar in functionality to Peripheral Activity detection register 0.

Perif_Act1

Access = 0022h/0023h

Regoffset = 06Ah

7	6	5	4	3	2	1	0
Rsv							
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved. Must be programmed to '0'.

POWER MANAGEMENT

18.2.12. ADDRESS RANGE 0 REGISTER 0

This register contains bits which are compared with PCI address bits 31-24 if range compare is enabled for memory cycle or compared against bits 15-8 if range compare is enabled for IO cycles.

<i>Add_Rang0-0</i>				Access = 0022h/0023h		Regoffset = 06Bh	
7	6	5	4	3	2	1	0
Default value after reset = 00h							

18.2.13. ADDRESS RANGE 0 REGISTER 1

Add_Rang0-1

Access = 0022h/0023h

Regoffset = 06Ch

7	6	5	4	3	2	1	0
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-3		These bits are compared with PCI address bits 23-19 if range compare is enabled for memory cycle, or compared against bits 7-3 if range compare is enabled for IO cycles.
Bit 2		This bit is compared with PCI address bit 18 if range compare is enabled for memory cycle, or compared with address bit 2 if range compare is enabled for IO cycles and range is 4-Bytes. Otherwise this bit when 1 specifies that the range of IO address to be compared is 16-Bytes and when 0, the range is 8-Bytes.
Bit 1		This bit is compared with PCI address bit 17 if range compare is enabled for memory cycle. Otherwise if range compare is enabled for IO cycles, this bit if 1 specifies that the range of IO address to be compared is 8/16-Bytes and when 0 the range is 4-Bytes.
Bit 0		This bit when '1' specifies that range compare should be done for memory cycles and when '0', for IO cycles.

POWER MANAGEMENT

18.2.14. SMI CONTROL REGISTER 0

This register controls the generation of an SMI, as follows:

<i>SMI_Cont0</i>				Access = 0022h/0023h		Regoffset = 071h	
7	6	5	4	3	2	1	0
							Rsv
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7		If '1' then generate SMI on Doze time-out. Otherwise if set to a '0', the hardware will transition to Doze state automatically on Doze time-out.
Bit 6		If '1' then generate SMI on Standby time-out. Otherwise if set to a '0', the hardware will transition to Standby state automatically on Standby time-out.
Bit 5		If '1' then generate SMI on Suspend time-out. Otherwise if set to a '0', SMI is not generated. The hardware never transitions into Suspend state by itself.
Bit 4		If '1' then generate SMI on House-keeping time-out. Otherwise if set to a '0', the hardware will automatically transition back to the doze or standby state (which ever state it was in before entering house-keeping state).
Bit 3		If '1' then generate SMI on detecting a house-keeping activity. Otherwise if set to a '0', and if in Doze or Standby state, the hardware will automatically transition to the associated house_keeping states for the duration programmed in the house-keeping timer.
Bit 2		If '1' then generate SMI on detecting a system activity. Otherwise if set to a '0', and if in Doze or Standby state, the hardware will automatically transition to Power-on state on detecting a unmasked system activity. This bit will typically be set to a '1' by software on entering a power-down state so that a system activity can wake up the system.
Bit 1		This is a write only bit. Setting this bit to a '1' sets bit-7 of the SMI status register 1 and generates an SMI. This bit however will always read back as '0'.
Bit 0	Rsv	Reserved.

18.2.15. SMI STATUS REGISTER 0

This register contains the status information pertaining to the SMI.

SMI_Stat0

Access = 0022h/0023h

Regoffset = 073h

7	6	5	4	3	2	1	0
DTO	STO	STO	HKT	HKA	SAD	PID	PAD
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	DTO	Doze time-out. This bit is set to a '1' when Doze time-out occurs. An SMI will be generated if associated SMI enable bit in SMI Control register is set to a '1'. The software must write this bit to a '1' to deassert SMI#. If SMI generation has been disabled then the controller will automatically transition to Doze state. This bit will then be cleared on transition from Doze or Standby to Power-on state.
Bit 6	STO	Standby time-out. This bit will be set to a '1' when Standby time-out occurs. An SMI will be generated if the associated SMI enable bit in SMI Control register is set to a '1'. The software must write this bit to a '1' to deassert SMI#. If SMI generation has been disabled then the hardware will automatically transition to Standby state. This bit will then be cleared on transition Standby to Power-on state.
Bit 5	STO	Suspend time-out. This bit will be set to a '1' when Suspend time-out occurs. An SMI will be generated if the associated SMI enable bit in the SMI Control register is set to a '1'. The software must write this bit to a '1' to deassert SMI#.
Bit 4	HKT	House-keeping timeout detected. This bit will be set to a '1' if the controller is in one of the house-keeping states and the house-keeping timer expires. An SMI will be generated if the associated SMI enable bit in the SMI Control register is set to a '1'. The software must write this bit to a '1' to deassert SMI#. If the SMI generation has been disabled, the hardware will automatically transition to doze or standby state. This bit then will be cleared on transition from Doze or Standby states to any other state.
Bit 3	HKA	House-keeping activity detected. This is a read-only bit and represents the OR of the System activity status registers masked (ANDed) with the corresponding bits in the House-keeping Activity enable registers. An SMI will be generated when this bit is a '1' and if the associated SMI enable bit in the SMI Control register is set to a '1'. The software can refer to Activity status register to determine the cause of the interrupt. The software must clear the corresponding bits of the Activity Status register to deassert SMI#. If SMI generation has been disabled and if the controller in Doze or Standby state, it will automatically transition to House-keeping state.

POWER MANAGEMENT

Bit Number	Mnemonic	Description
Bit 2	SAD	System Activity detected. This is a read-only bit and represents the OR of the System activity Status registers masked (ANDed) with the corresponding bits of the System Activity enable registers. An SMI will be generated if this bit is a '1' and if the associated SMI enable bit in SMI Control register is set to a '1'. The software can refer to Activity status register to determine the cause of this interrupt. The software must clear the System Activity Status registers bits for the enabled system activities to deassert SMI#. If SMI generation has been disabled and if the controller is in Doze or Standby state, it will automatically transition to Power-on state.
Bit 1	PID	Peripheral Inactivity detected. This is a read-only bit and represents the OR of Peripheral Inactivity Status register bits masked (ANDed) with the associated Peripheral inactivity detection register bit. An SMI# will be generated when this bit is a '1'. The software can refer to Peripheral Inactivity status registers to determine which peripheral should be powered down. The software must clear the corresponding bits of the Peripheral Inactivity detection register to deassert SMI#.
Bit 0	PAD	Peripheral Activity Detected. This is a read-only bit and represents the OR of the System activity Status register masked (ANDed) with the corresponding bits of the Peripheral Activity detection registers. An SMI will be generated when this bit is a '1'. The software can refer to the System Activity status register to determine which peripheral caused the interrupt. The software must clear the corresponding bits of the System activity register to deassert SMI#.

Programming notes:

The SMI# output is a logical OR of all the bits (ANDed with their respective SMI generation enable bits) in this register. SMI# output will be deasserted within 3 PCI clocks after the cause of the SMI# is cleared. This register defaults to 00h after reset deasserting SMI# output.

18.2.16. SMI STATUS REGISTER 1

This register is similar to SMI Status register 0 in that it reports the cause of the SMI to the software.

SMI_Stat1

Access = 0022h/0023h

Regoffset = 074h

7	6	5	4	3	2	1	0
S SMI	Rsv						
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	S SMI	Software SMI. This bit is set to a '1' by write writing a '1' in bit-1 of the SMI Control register. The software must clear this bit to deassert SMI#.
Bits 6-0	Rsv	Reserved.

POWER MANAGEMENT

18.2.17. PERIPHERAL INACTIVITY STATUS REGISTER 0

This register contains a '1' in a bit position if the associated peripheral was inactive for the entire duration of the last peripheral time-out period.

Perif_Stat0			Access = 0022h/0023h			Regoffset = 075h	
7	6	5	4	3	2	1	0
PIO	SIO	KBD	FDC	HDC	ARO	Rsv	
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	PIO	Parallel port (PIO) activity.
Bit 6	SIO	Serial port (SIO) activity.
Bit 5	KBD	Keyboard (KBD) activity.
Bit 4	FDC	Floppy Disk Controller (FDC) activity.
Bit 3	HDC	Hard Disk Controller (HDC) activity.
Bit 2	ARO	Address range 0
Bits 1-0	Rsv	Reserved.

It can also be cleared by software by writing a '1' in the bit which is set to '1'.

Programming notes:

A bit in this register is set to a '1' only at peripheral timer time-out. It is set to a '0' as soon as an activity from the associated peripheral is detected.

The status reflected in this register is not conditioned by whether or not the peripheral was enabled for inactivity detection through the Peripheral Inactivity Detection registers. The SMI however will be generated only if any of the enabled peripherals (via Peripheral Inactivity Enable register) were inactive for the entire duration of the peripheral time out.

18.2.18. ACTIVITY STATUS REGISTER 0

This register records presence of activity.

Activ_Stat0

Access = 0022h/0023h

Regoffset = 077h

7	6	5	4	3	2	1	0
DRQ	PCIM	PIO	SIO	KBD	FDC	HDC	Rsv
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	DRQ	DMA Request (DRQ) activity.
Bit 6	PCIM	PCI master device (PCIM) activity.
Bit 5	PIO	Parallel IO (PIO) activity.
Bit 4	SIO	Serial IO (SIO) activity.
Bit 3	KBD	Keyboard (KBD) activity.
Bit 2	FDC	Floppy Disk Controller (FDC) activity.
Bit 1	HDC	Hard Disk Controller (HDC) activity.
Bit 0	Rsv	Reserved.

Programming notes:

A '1' in a bit position indicates that presence of the associated activity since the bit was last cleared. Once set, a bit of this register can only be cleared by software writing a '1' to it or by reset or if auto power management is enabled then any transition to Doze or Standby state (including the ones from house-keeping states) will clear all enabled System and House-keeping activities.

The status reflected in this register is not conditioned by the settings of System Activity Enable, House-keeping Activity Enable, Peripheral Inactivity or Peripheral Activity Detection registers.

POWER MANAGEMENT

18.2.19. ACTIVITY STATUS REGISTER 1

This register is similar to Activity Status register 0. It contains the status for the following bits.

Activ_Stat1

Access = 0022h/0023h

Regoffset = 078h

7	6	5	4	3	2	1	0
Rsv		AR0	Rsv				
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-6	Rsv	Reserved. Must be programmed to '0'
Bit 5	AR0	Address range 0
Bits 4-0	Rsv	Reserved. Must be programmed to '0'

18.2.20. ACTIVITY STATUS REGISTER 2

This register is similar to Activity Status registers 0 and 1.

Activ_Stat2

Access = 0022h/0023h

Regoffset = 079h

7	6	5	4	3	2	1	0
IRQ15-1	IRQ0	NMI	Rsv				
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	IRQ15-1	IRQ15-1 activity.
Bit 6	IRQ0	IRQ0 activity.
Bit 5	NMI	NMI activity.
Bits 4-0	Rsv	Reserved.

POWER MANAGEMENT

18.2.21. PMU STATUS REGISTER

This register contains the state the power management controller currently is in.

<i>PMU</i>			Access = 0022h/0023h			Regoffset = 07Ah	
7	6	5	4	3	2	1	0
Rsv	PMU	PMU	PMU	PMU	PMU	PMU	PMU
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved.
Bit 6	PMU	PMU microsecond clock test mode. This bit is for factory use only and must be set to a '0' by the software. Setting this bit to a 1' causes the microsecond clock to tick at oscillator clock frequency instead of every microsecond.
Bit 5	PMU	PMU millisecond clock test mode. This bit is for factory use only and must be set to a '0' by the software. Setting this bit to a 1' causes the millisecond clock to tick at oscillator clock frequency instead of every millisecond.
Bit 4	PMU	PMU second clock test mode. This bit is for factory use only and must be set to a '0' by the software. Setting this bit to a 1' causes the second clock to tick at oscillator clock frequency instead of every second.
Bit 3	PMU	PMU minute clock test mode. This bit is for factory use only and must be set to a '0' by the software. Setting this bit to a 1' causes the minute clock to tick at oscillator clock frequency instead of every minute.
Bit 2	PMU	PMU state (see Table 18-7).
Bit 1	PMU	PMU state (see Table 18-7).
Bit 0	PMU	PMU state (see Table 18-7).

Table 18-7. PMU State

Bit 2	Bit 1	Bit 0	PMU state
0	0	0	Power-on
0	0	1	Doze
0	1	0	Standby
0	1	1	Suspend
1	0	1	Doze_house_keeping
1	1	0	Standby_house_keeping
1	1	1	Reserved

The architecture allows for: (1) the software to explicitly program the power-down state of the controller, or (2) the controller can change states automatically (auto-power down mode of operation), or (3) a mix of the two. Some power-down states are entered and exited automatically by the hardware, while others require software assist. This is based on the SMI Control register settings as follows:

Transition from Power-on to Doze state will take place automatically on Doze time-out, if bit-7 of the SMI control register is set to a '0'. Otherwise if bit-7 is programmed to be a '1', an SMI will be generated and the software can change the state to Doze.

Transition from Doze to Power-on will take place automatically in the presence of an enabled system activity if bit-2 of the SMI control register is programmed to '0'. Otherwise if bit-2 is programmed to a '1', an SMI will be generated and software can change the state to Power-on.

Transition from Doze to Doze_house_keeping state will take place automatically if an enabled house_keeping activity is detected and bit-4 of the SMI control register is set to a '0'. Otherwise if bit-7 is programmed to be a '1', an SMI will be generated.

Transition from Doze_house_keeping state to Doze will take place automatically on house-keeping time-out if bit-3 of the SMI control register is set to a '0'. Otherwise an SMI will be generated.

Transition from Doze_house_keeping state to Power-on will take place on detecting an enabled system activity automatically if bit-2 of the SMI control register is programmed to '0'. Otherwise an SMI will be generated.

Transitions from Doze or Power-on state to Standby will take place automatically on standby time-out if bit-6 of the SMI control register is set to a '0'. Otherwise an SMI will be generated.

Transition from Standby to Power-on will take place automatically in presence of an enabled system activity if bit-2 of the SMI control register is programmed to be a '0'. Otherwise if bit-2 is programmed to a '1', an SMI will be generated and software can change the state to Power-on.

Transition from Standby to Standby_house_keeping state will take place automatically if an enabled house_keeping activity is detected and bit-4 of the SMI control register is set to a '0'. Otherwise if bit-7 is programmed to be a '1', an SMI will be generated.

Transition from Standby_house_keeping state to Standby will take place automatically on house-keeping time-out if bit-3 of the SMI control register is set to a '0'. Otherwise an SMI will be generated.

Transition from Standby_house_keeping state to Power-on will take place on detecting an enabled system activity automatically if bit-2 of the SMI control register is programmed to '0'. Otherwise SMI interrupt will be generated.

The hardware never transitions to Suspend state automatically.

The power saving features associated with each power-down state are independent of how the state was entered.

POWER MANAGEMENT

18.2.22. GENERAL PURPOSE REGISTER

This is a read/write IO register that can be used by software.

GP

Access = 0022h/0023h

Regoffset = 07Bh

7	6	5	4	3	2	1	0
GP	GP	GP	GP	GP	GP	GP	GP
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bit 7	GP	General Purpose Register Bit 7.
Bit 6	GP	General Purpose Register Bit 6.
Bit 5	GP	General Purpose Register Bit 5.
Bit 4	GP	General Purpose Register Bit 4.
Bit 3	GP	General Purpose Register Bit 3.
Bit 2	GP	General Purpose Register Bit 2.
Bit 1	GP	General Purpose Register Bit 1.
Bit 0	GP	General Purpose Register Bit 0.

Programming notes:

Writing to this register also updates the external '373 latch that can be used to control external devices for power-down purposes. Reads of this register return the value of this internal register.

The GPIOCS# signal will be asserted when writing to this register to latch the data on the ISA data bus.

18.2.23. CLOCK CONTROL REGISTER 0

This register allows control over power saving via stop clock modulation. The power-saving can be tuned to the power-management state the PMU is in.

Clk_Cont0

Access = 0022h/0023h

Regoffset = 07Ch

7	6	5	4	3	2	1	0
STPCLK			DSSS			STPCLK	Rsv
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-5	STPCLK	Power-on and housekeeping states STPCLK# modulation control. These bits control the duty cycle of STPCLK# deassertion when the PMU is in Power-on or one of the house-keeping states given in Table 18-8 . The STPCLK# is deasserted and the duty-cycle control ignored if an SMI is pending.
Bit 4-2	DSSS	Doze/Standby/Suspend states STPCLK# modulation control. These bits control the duty cycle of the STPCLK# deassertion when PMU is in one of the power-down states as given in Table 18-9 . The STPCLK# is deasserted and the duty-cycle control ignored if an SMI is pending.
Bit 1	STPCLK	STPCLK# modulation period. If '1' then the period is 64ms else, if '0', then the period is 64μs.
Bit 0	Rsv	Reserved.

Table 18-8. Power-on and Housekeeping States

Bit 7	Bit 6	Bit 5	Ratio	Power-on STPCLK# Modulation
0	0	0	1	STPCLK# is never asserted
0	0	1	1/2	1 half period
0	1	0	1/4	1 quarter period
0	1	1	1/8	one-eighth period
1	0	0	1/16	one-sixteenth period
1	0	1	1/32	1/32 period
1	1	0	1/64	1/64 period
1	1	1		Reserved.

Table 18-9. Doze/Standby/Suspend States

Bit 4	Bit 3	Bit 2	Ratio	Doze STPCLK# Modulation
0	0	0	1	STPCLK is never asserted
0	0	1	1/2	1 half period
0	1	0	1/4	1 quarter period
0	1	1	1/8	one-eighth period
1	0	0	1/16	one-sixteenth period
1	0	1	1/32	1/32 period
1	1	0	1/64	1/64 period
1	1	1	0	The entire period

18.2.24. DOZE TIMER READ BACK REGISTER

This read only register is provided for test purposes to read back the current value of the upper 8-bits of the 9-bit doze timer.

<i>Doze</i>		Access = 0022h/0023h				Regoffset = 088h	
7	6	5	4	3	2	1	0
Default value after reset = 00h							

Bit Number	Mnemonic	Description
Bits 7-0		Bits 8-1 of the current value of the doze timer.

Programming notes:

This register should not be used by the software.

Note that bit 0 of the current value of the doze timer is not readable.

POWER MANAGEMENT

18.2.25. STANDBY TIMER READ BACK REGISTER

This read only register is provided for test purposes to read back the current value of 5-bit standby timer.

Standby

Access = 0022h/0023h

Regoffset = 089h

7	6	5	4	3	2	1	0
Rsv							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-5	Rsv	Reserved.
Bits 4-0		Bits 4-0 of the current value of the standby timer.

Programming notes:

This register should not be used by software.

18.2.26. SUSPEND TIMER READ BACK REGISTER

This read only register is provided for test purposes to read back the current value of the 7-bit Suspend timer.

Suspend

Access = 0022h/0023h

Regoffset = 08Ah

7	6	5	4	3	2	1	0
Rsv							
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bit 7	Rsv	Reserved.
Bits 6-0		Bits 6-0 of the current value of the suspend timer.

Programming notes:

This register should not be used by software.

POWER MANAGEMENT

18.2.27. HOUSE-KEEPING TIMER READ BACK REGISTER

This read only register is provided for test purposes to read back the current value of the upper 8-bits of the 9-bit house-keeping timer.

<i>HK_Timer</i>		Access = 0022h/0023h				Regoffset = 08Bh	
7	6	5	4	3	2	1	0
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0		Bits 8-1 of the house-keeping timer.

Programming notes:

This register should not be used by software.

18.2.28. PERIPHERAL TIMER READ BACK REGISTER

This read only register is provided for test purposes to read back the current value of the upper 8-bits of the 9-bit Peripheral timer.

Perif_Timer

Access = 0022h/0023h

Regoffset = 08Ch

7	6	5	4	3	2	1	0
Default value after reset = undefined							

Bit Number	Mnemonic	Description
Bits 7-0		Bits 8-1 of the Peripheral timer.

Programming notes:

This register should not be used by software.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© 2000 STMicroelectronics - All Rights Reserved

The ST logo is a registered trademark of STMicroelectronics.

All other names are the property of their respective owners.

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.

